Technological Innovations in Frequency Distribution over DSL

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What this presentation is all about?

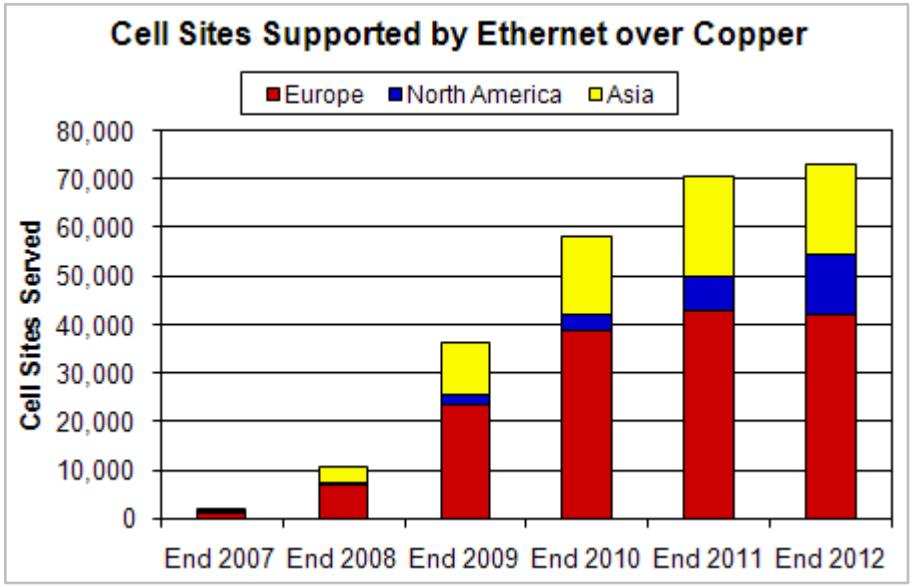
I would like to put the focus on rather "painful" problem that is timing distribution over last-mile DSL links

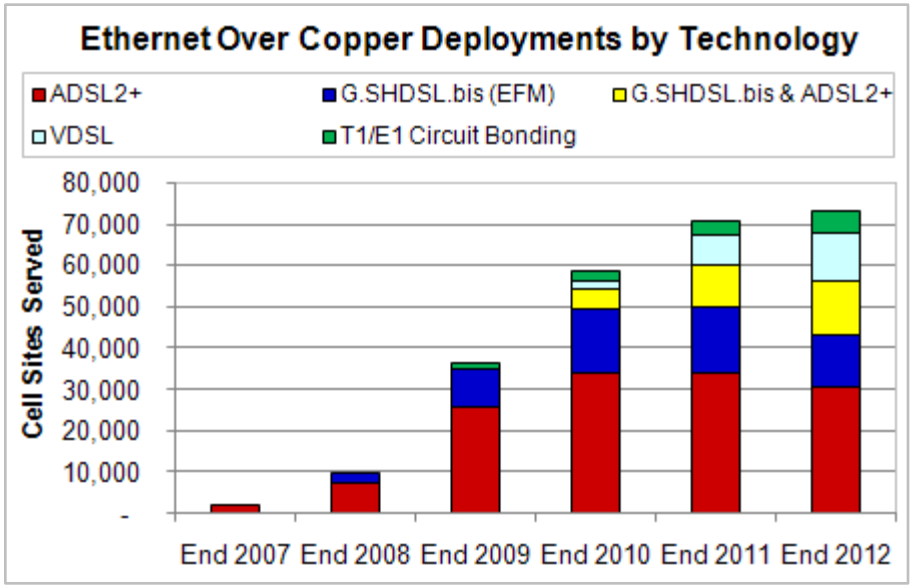
DSLs have an inherit standardized (but not mandatory) mechanism to distribute frequency called Network Timing Reference (NTR)

Unfortunately, many new DSLAMs (especially IP DSLAMs) do not support it

This presentation will show that a very low-cost additional piece of equipment near the DSLAM can totally solve the problem, while significantly reducing the cost of the current ACR based CPEs

Cellular operator demand for Ethernet over Copper*

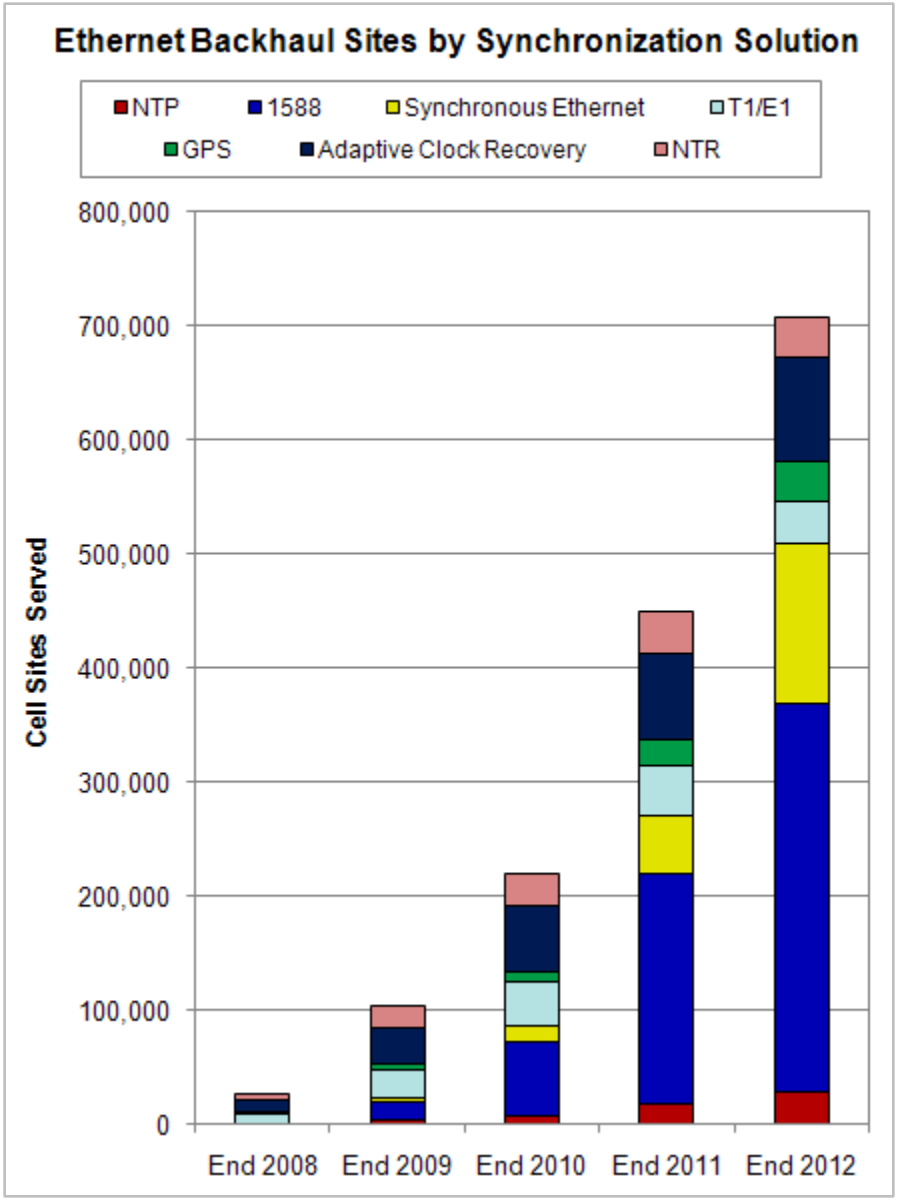




- "We expect deployments to be concentrated in the next two years and to remain in place for three or four years once deployed."
- "Europe will account for at least 60% of the installed base of the world's Ethernet Over Copper backhaul deployments throughout the forecast period."
- "We believe there is potential for strong growth in EoC in North America by virtue of the market's unusually high present-day dependence on copper."

* Information extracted from Heavy Reading's "Ethernet Backhaul Market Tracker", July 2008.

Synchronization approaches to Ethernet Backhaul *

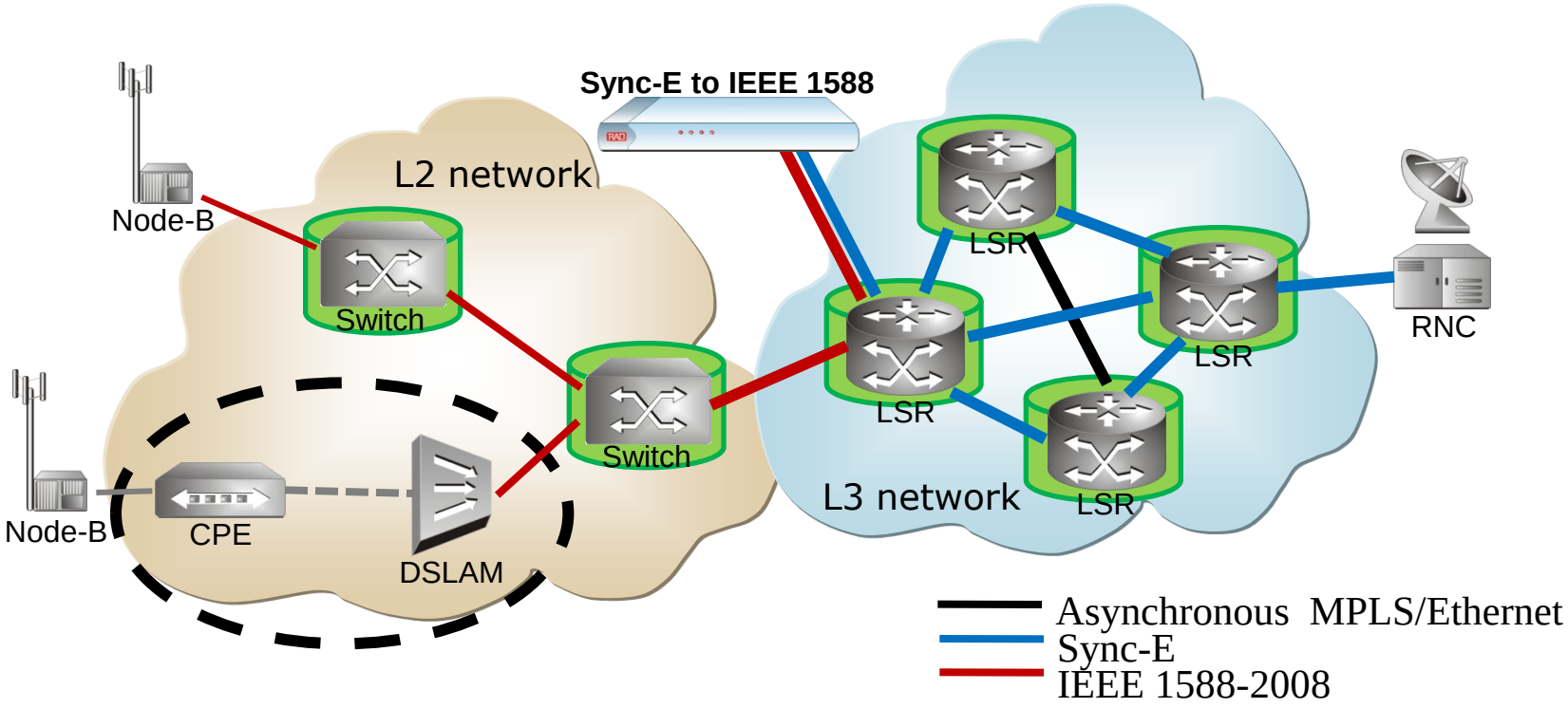


- "The predominant approaches to Ethernet backhaul synchronization in the immediate future will continue to be proprietary **Adaptive Clock Recovery** (ACR)"

- "NTR is a timing standard which is native to the DSL family of standards. Throughout we have assumed that **only 50% of EoC backhaul deployments are based on NTR**. This is due to market feedback that some EoC vendors have not yet implemented NTR effectively."

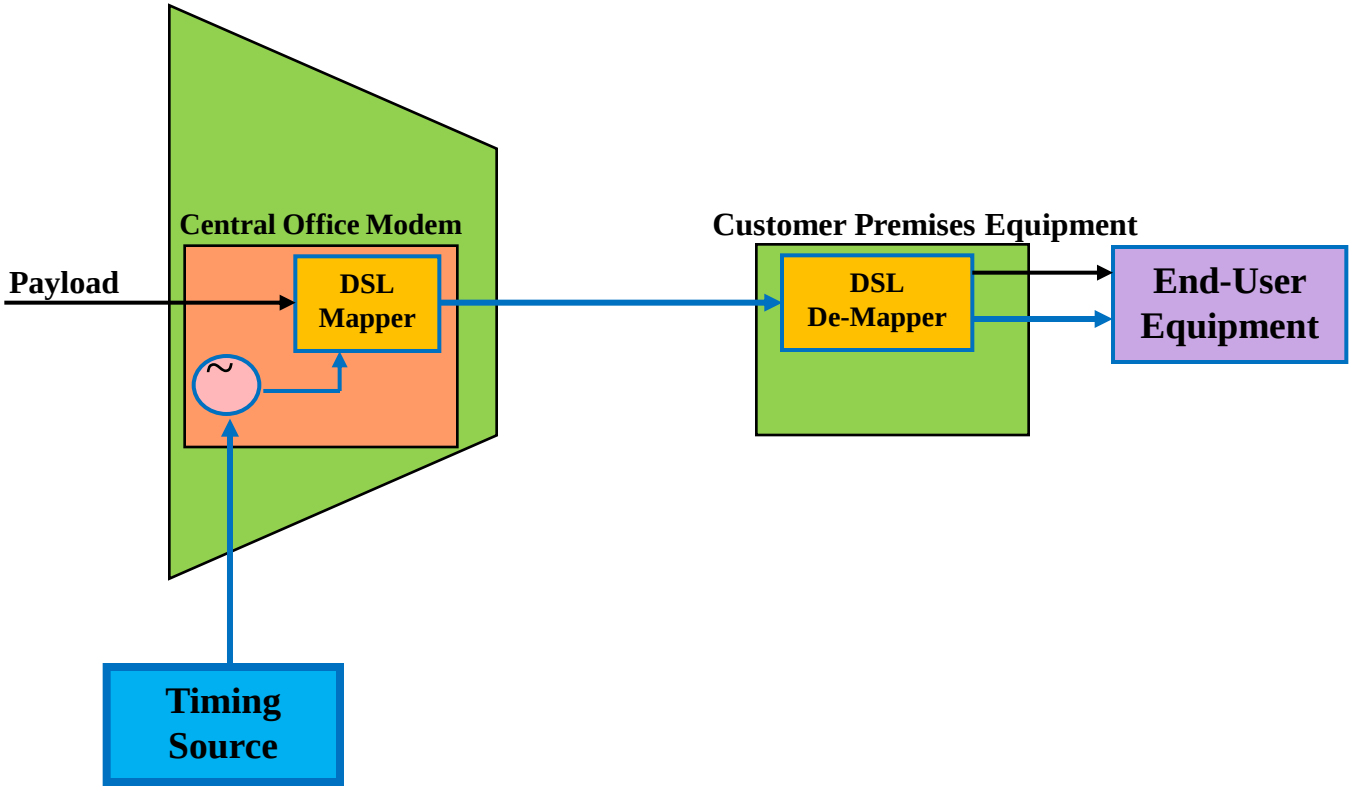
* Information extracted from Heavy Reading's "Ethernet Backhaul Market Tracker", July 2008.

Let's talk about DSL



While existing standardized solutions such as IEEE 1588v2 or Synchronous Ethernet are addressing the backhaul network, the last mile (that often introduces the greatest challenge) is overlooked

DSL – sometimes NTR is supported

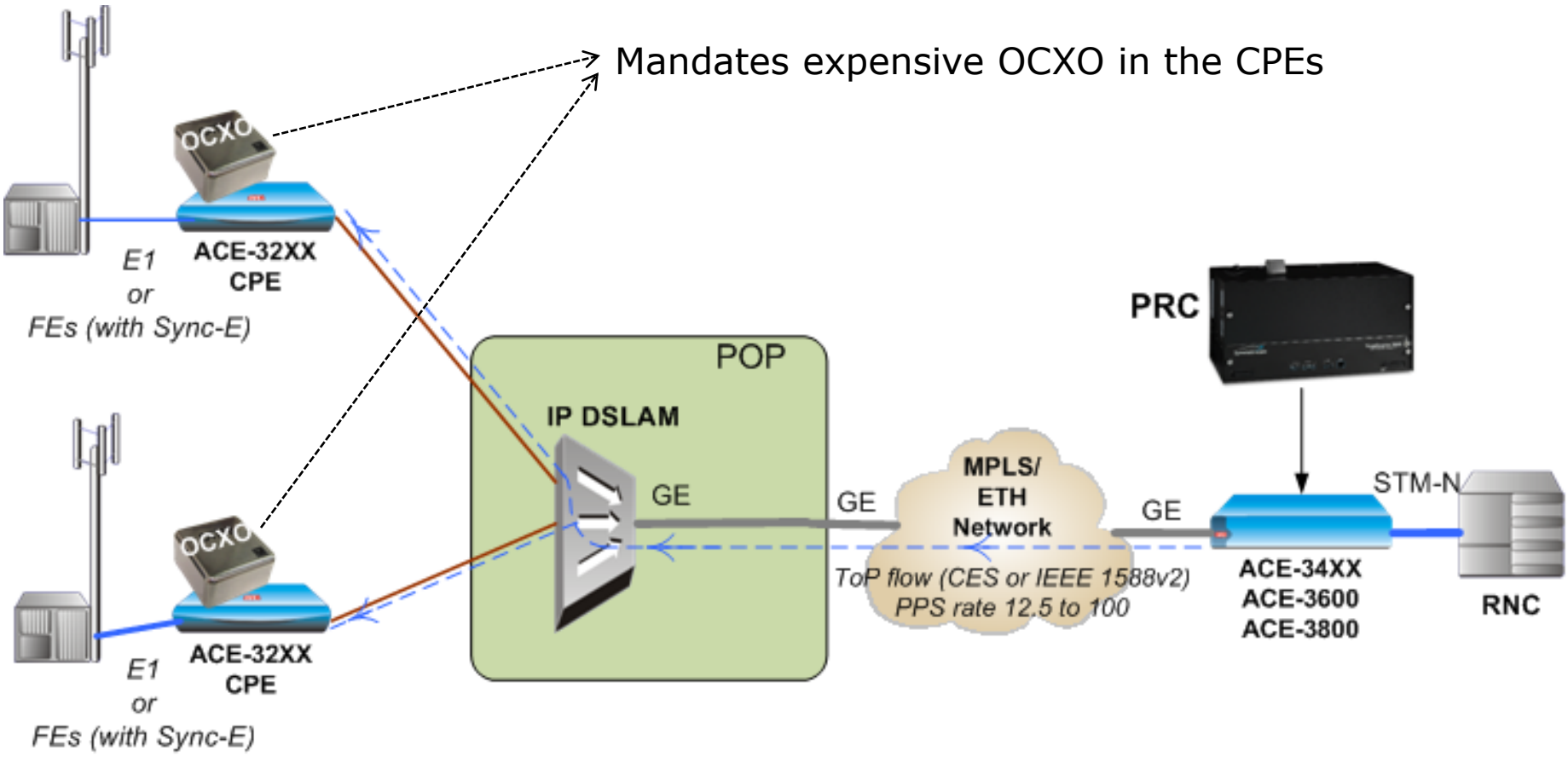


The Problem:

Many currently deployed DSLAMs (especially IP-DSLAMs) Do Not Support NTR!

DSL – often NTR is not supported

ACR (either using Timing PW or IEEE 1588v2) is currently the technology of choice for distributing frequency over DSL lines that don't support NTR



Problems with ACR in DSL (IEEE 1588v2 or CES)

- It often requires an expensive OCXO at the CPE

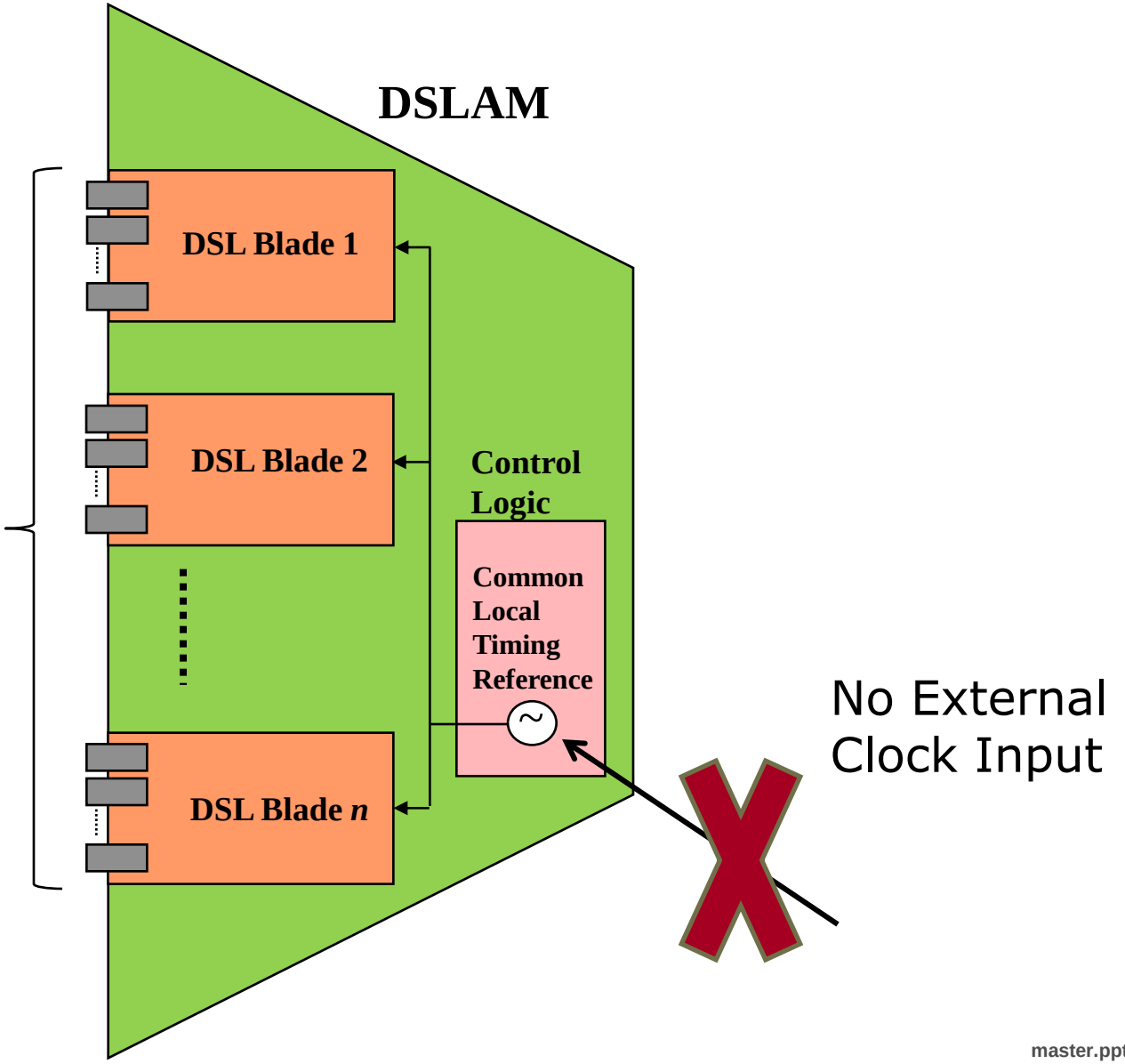
- It mandates a rather high (100 PPS) timing flow rate for best timing distribution performance

- Clock recovery performance is often Traffic Interface rather than Synchronization Interface as a consequence of excessive PDV introduced by the DSL link (especially low frequency components)

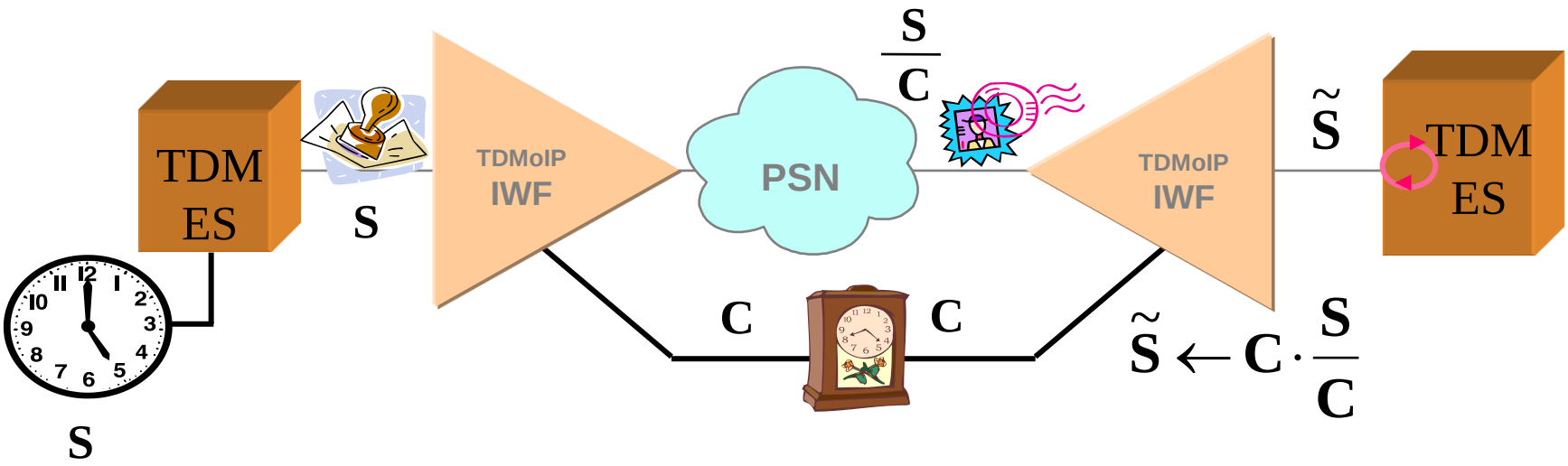
Architecture of non-NTR-supporting DSLAM

BUT:
All ports are timed from the same clock →

A "Common Clock"



A very efficient way to exploit common clocks → Differential scheme



- common clock is unrelated to TDM source clock. May be distributed over any infrastructure (e.g. physical-layer, GPS)
- **needn't be G.811 traceable**, as long as both IWFs see the same clock
- Source IWF timestamps each outgoing packet using the common clock. Destination IWF regenerates the original clock by comparing the timestamp of the incoming packet to a local representation based on the same common clock
- common clock makes PSN's PDV irrelevant, performance will **always** conform to the standards

RAD's High quality timing distribution over DSL

- New patent-pending technology that enables PRC-quality clock distribution over non-NTR supporting DSL links
- Clock quality (over the DSL link) is not affected by higher layer impairments such as Packet Delay Variation (PDV) and Packet Loss (PL)
- CPE devices require TCXO (ST3/4) rather than a costly OCXO (ST3E)
- Usually requires an additional **DSL PHY clock 'sniffing'** device near the DSLAM (i.e. DSL timing distributer) connected to one available DSLAM port. **Absolutely no change is necessary for the DSLAM HW**!
- Three supported clock distribution strategies:
  (I) PRC/BITS clock located in the POP (near the DSLAM)
  (II) PRC/BITS clock located in the end-application
  (III) PRC/BITS clock located at a remote location in the network

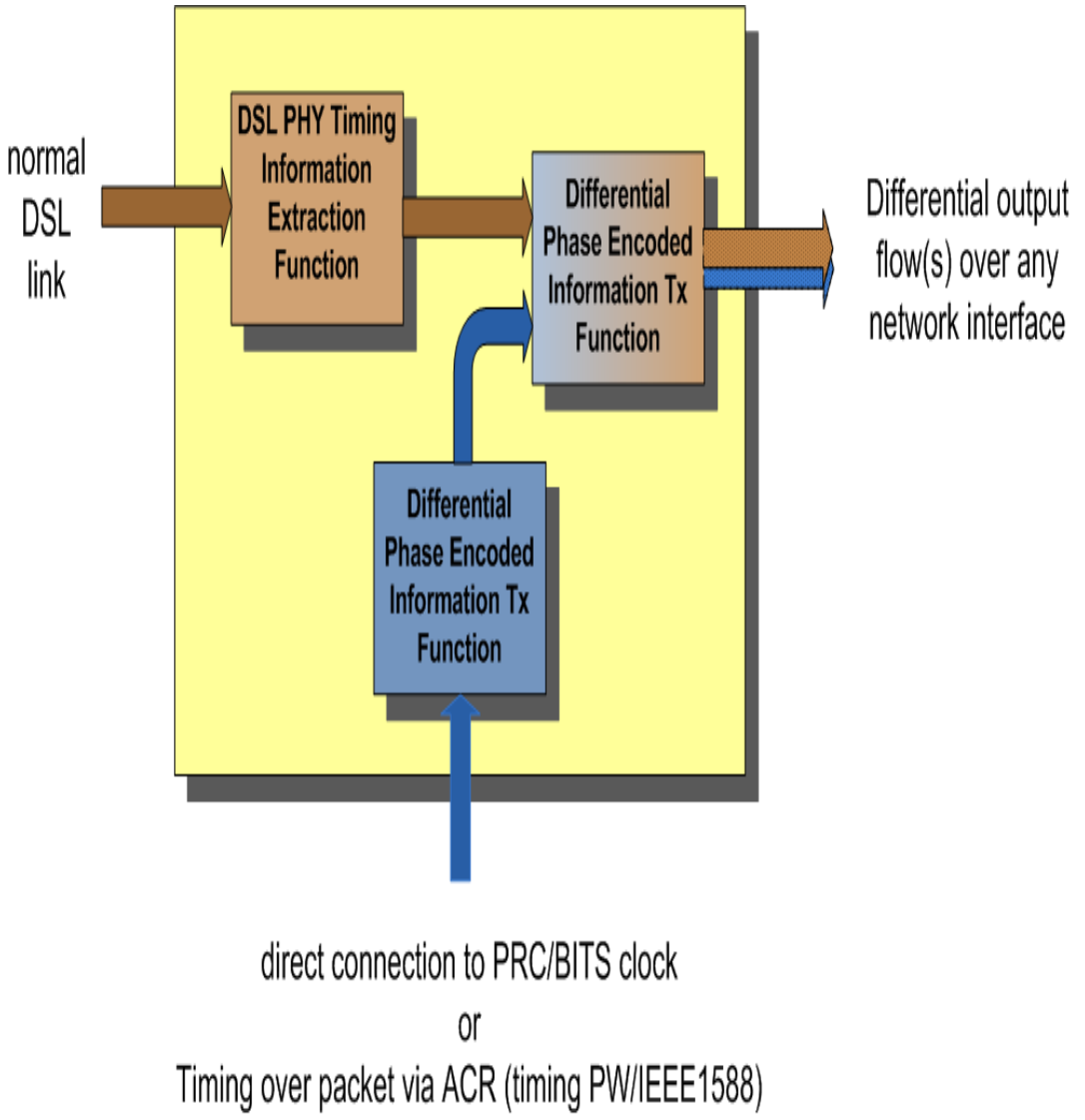
What is a DSL 'sniffer' device?

The sniffer has <u>always</u> **three logical connections** to other devices, namely

a) a first input connection, which is typically a DSL port, from which it observes the DSLAM's LTR clock

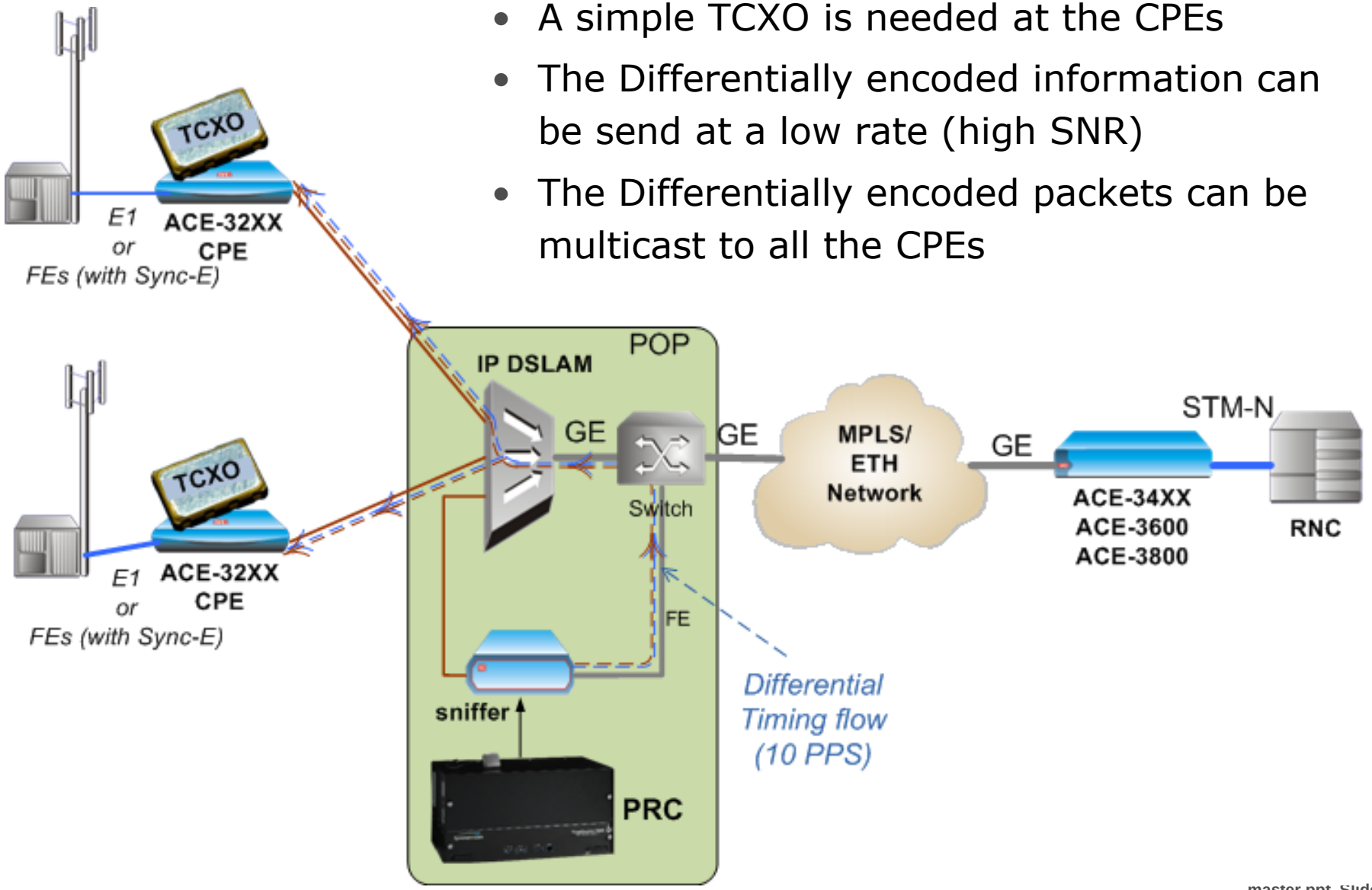
b) a second input connection, either a direct clock connection or a network connection, from which it directly or indirectly observes the PRC clock

c) an output connection, typically a network connection, to which it forwards timing packets containing encoded phase difference information

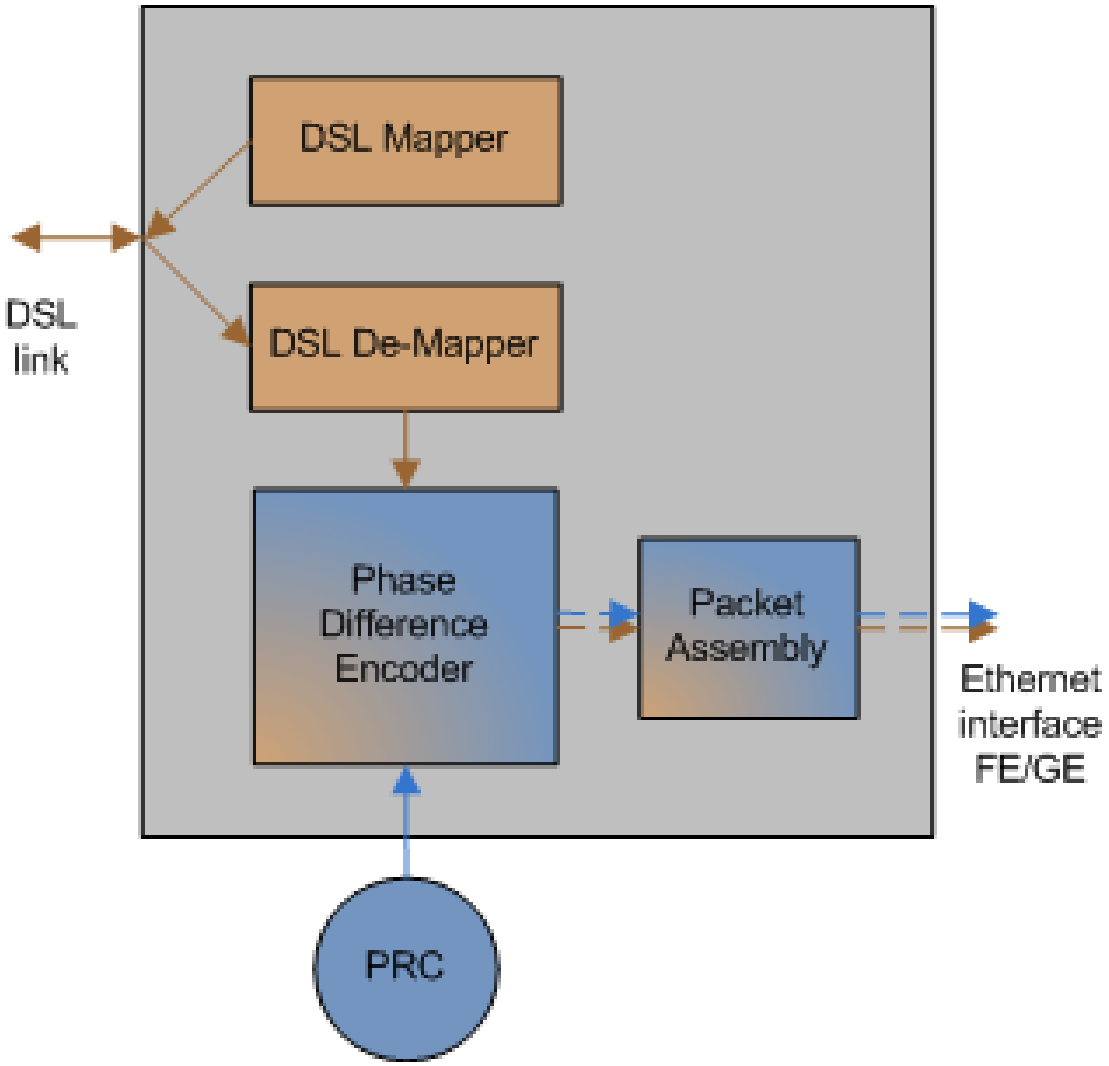


Clock distribution strategy I: PRC/BITS at the POP

- A simple TCXO is needed at the CPEs
- The Differentially encoded information can be send at a low rate (high SNR)
- The Differentially encoded packets can be multicast to all the CPEs



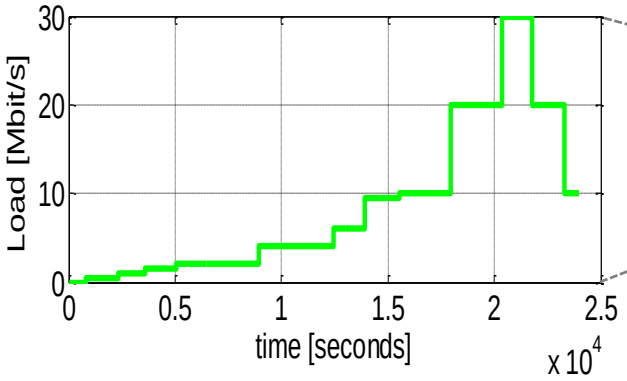
Examples of DSL 'sniffers' (I)



- The classic approach. Used when there is a PRC/BITS clock in the proximity of the DSLAM

- The DSL sniffer has 3 physical ports:
  1. DSL link input (to extract the DSL PHY clock)
  2. PRC direct input
  3. Network output interface

Clock distribution strategy I: real-world conditions lab test



IXIA 400T
Traffic generator

2.048 Mbit/s

Spirent
DLS-400S
SHDSL line
simulator

TCXO

FE

GE

GE

ACE-3400

switch

1.5 Km ETSI loop # 2

ACE-32XX
CPE

Sniffer + ACE 32XX CPE

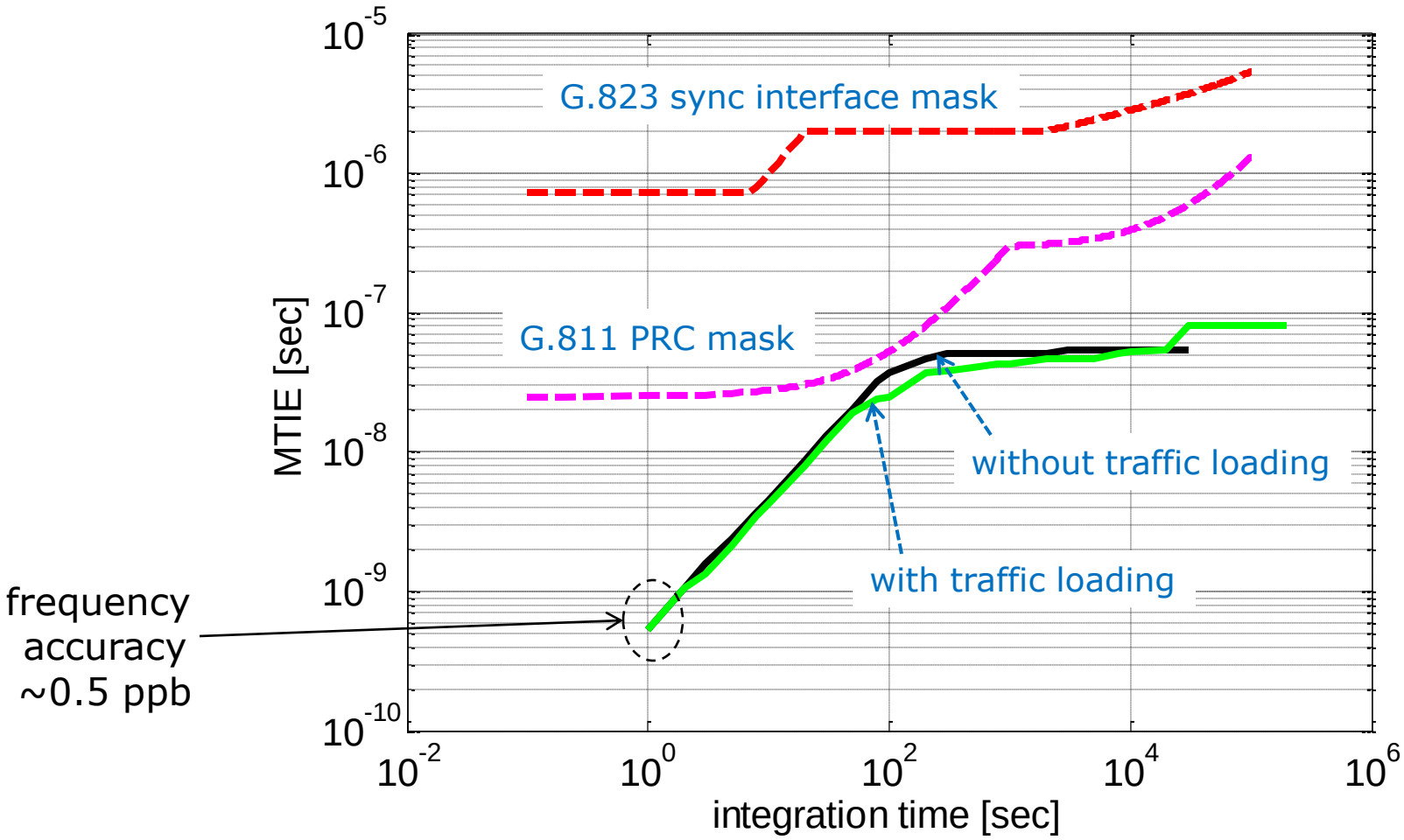
IP DSLAM
with
G.SHDSL cards

2.048MHz
ref.

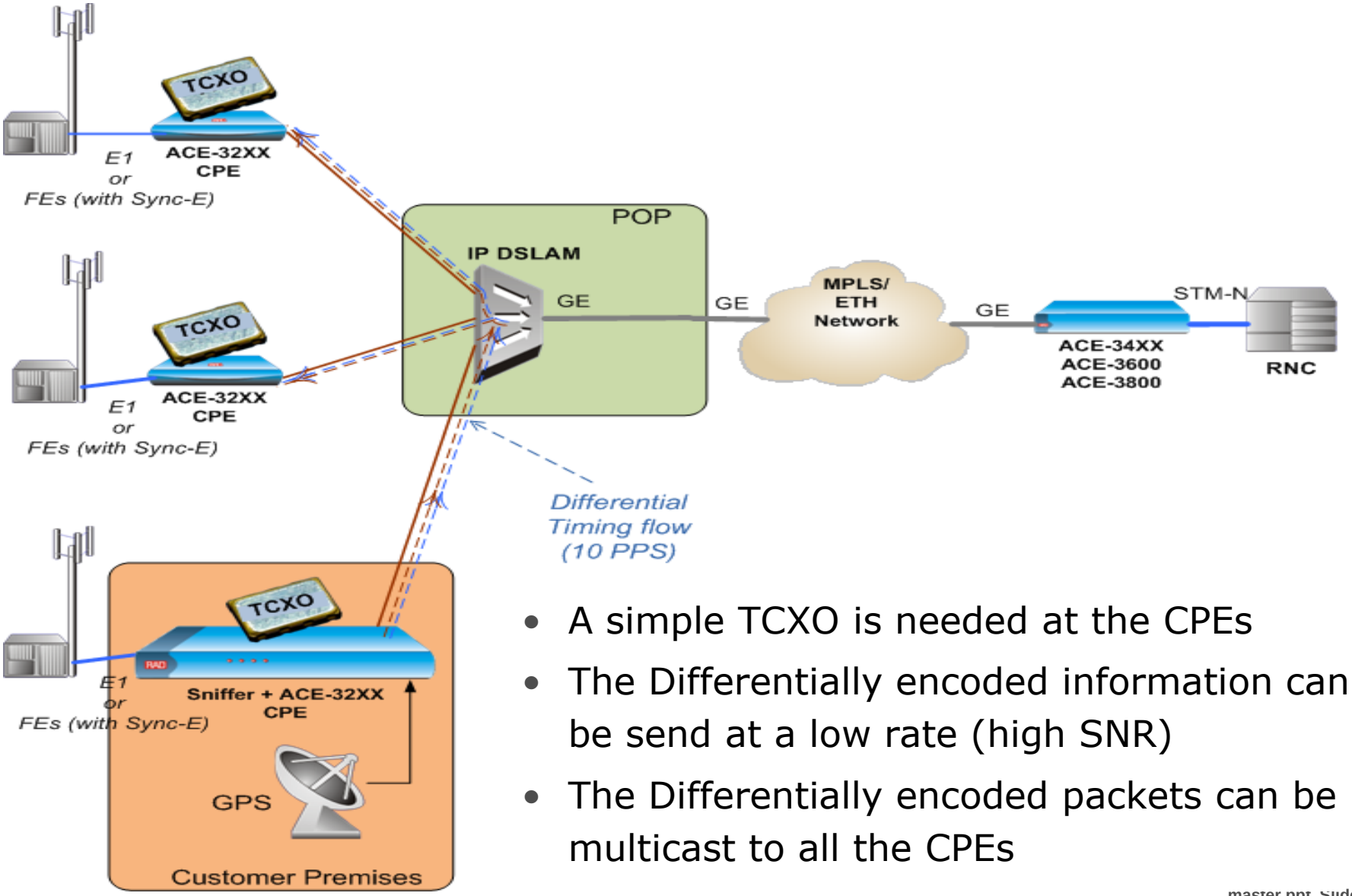
PRC

wander
analyzer

Clock distribution strategy I: clock recovery tests results

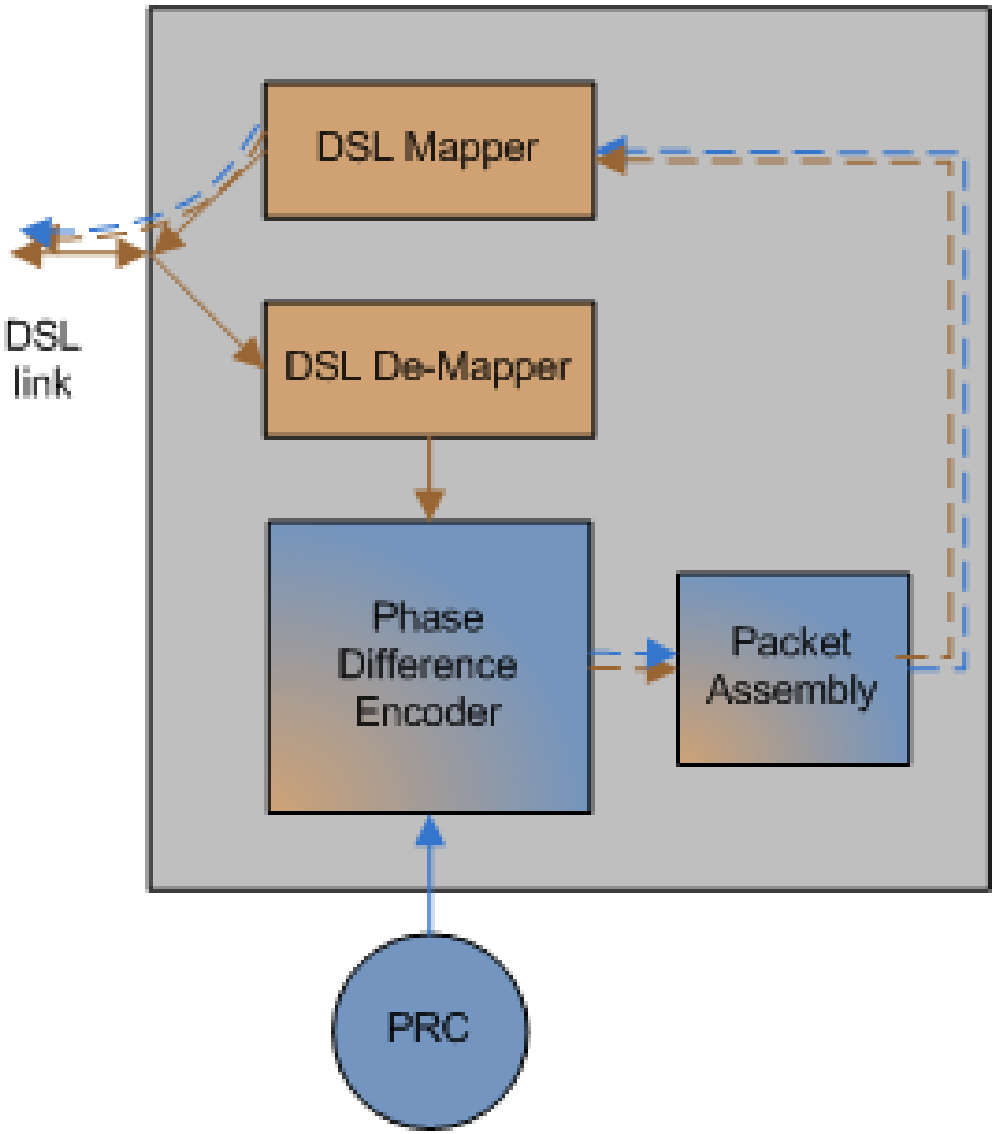


Clock distribution strategy II: PRC/BITS near the CSG (end device)



- A simple TCXO is needed at the CPEs
- The Differentially encoded information can be send at a low rate (high SNR)
- The Differentially encoded packets can be multicast to all the CPEs

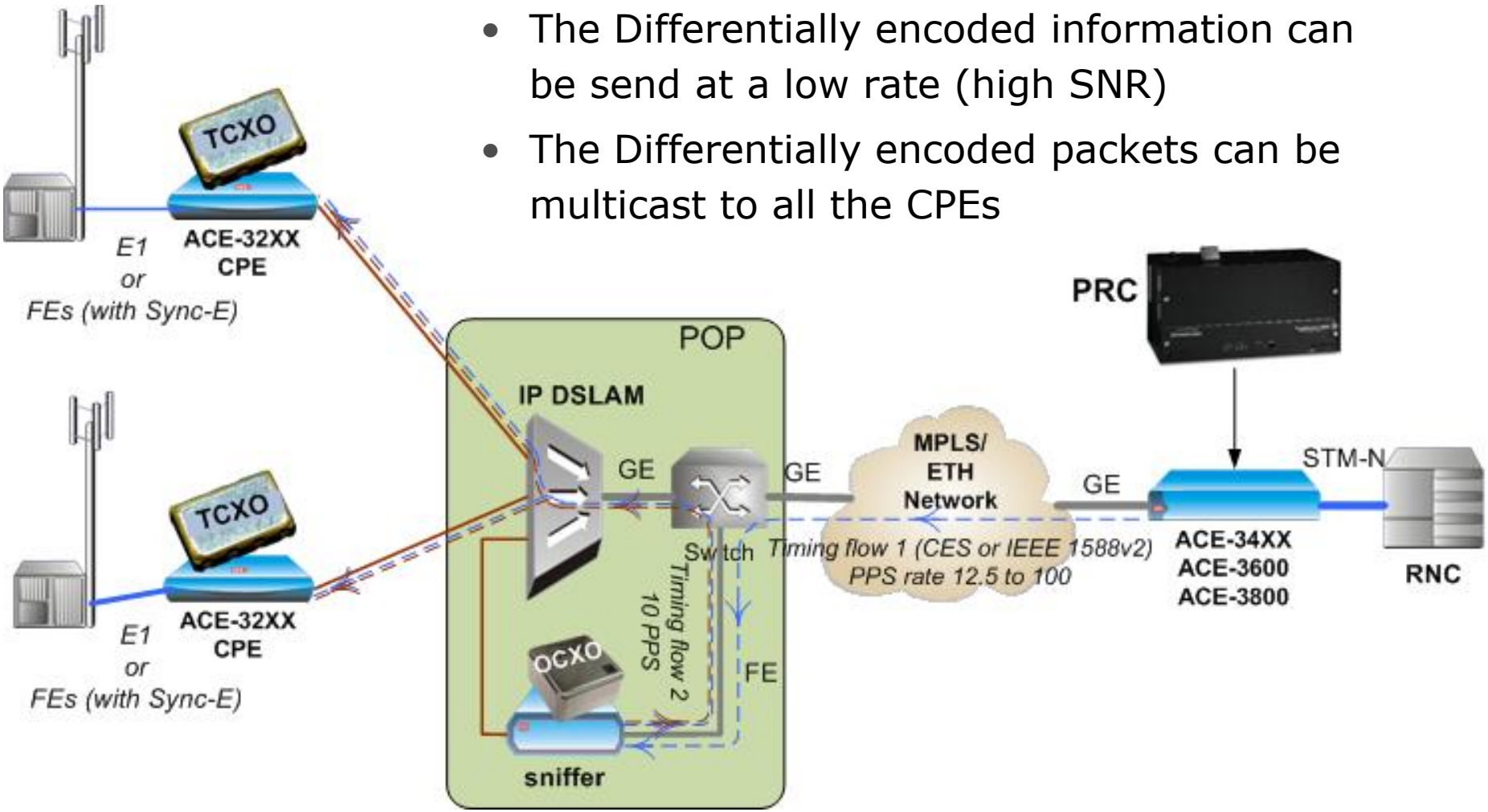
Examples of DSL 'sniffers' (II)



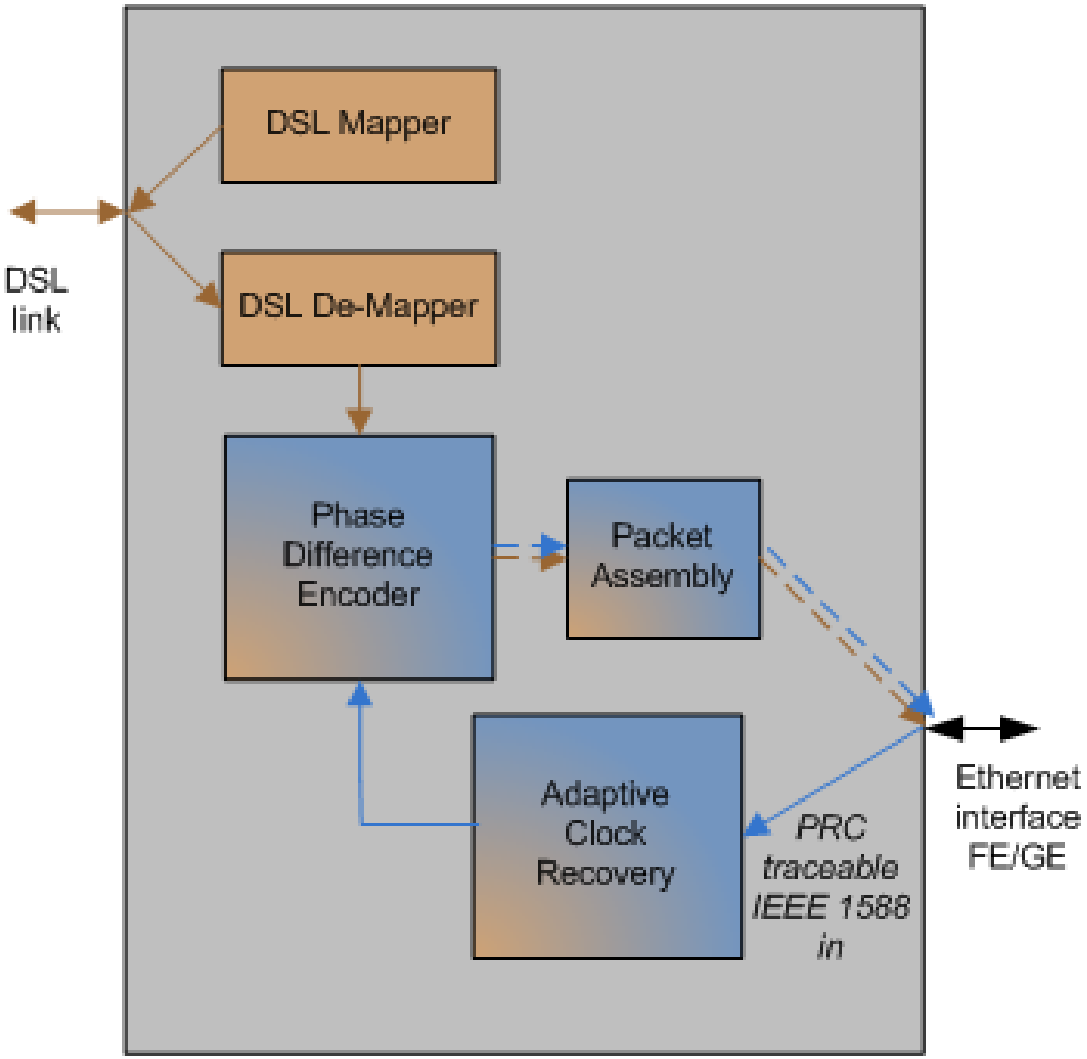
- Used when there is a PRC clock (usually a GPS) in the proximity of the end application
- The DSL sniffer has 2 physical ports:
  1. DSL link input/output (to extract the DSL PHY clock and Tx the Differentialy encoded information)
  2. PRC (GPS) ref. direct input

Clock distribution strategy III: PRC/BITS at a remote location

- A simple TCXO is needed at the CPEs
- An OCXO is usually needed at the sniffer
- The Differentially encoded information can be send at a low rate (high SNR)
- The Differentially encoded packets can be multicast to all the CPEs

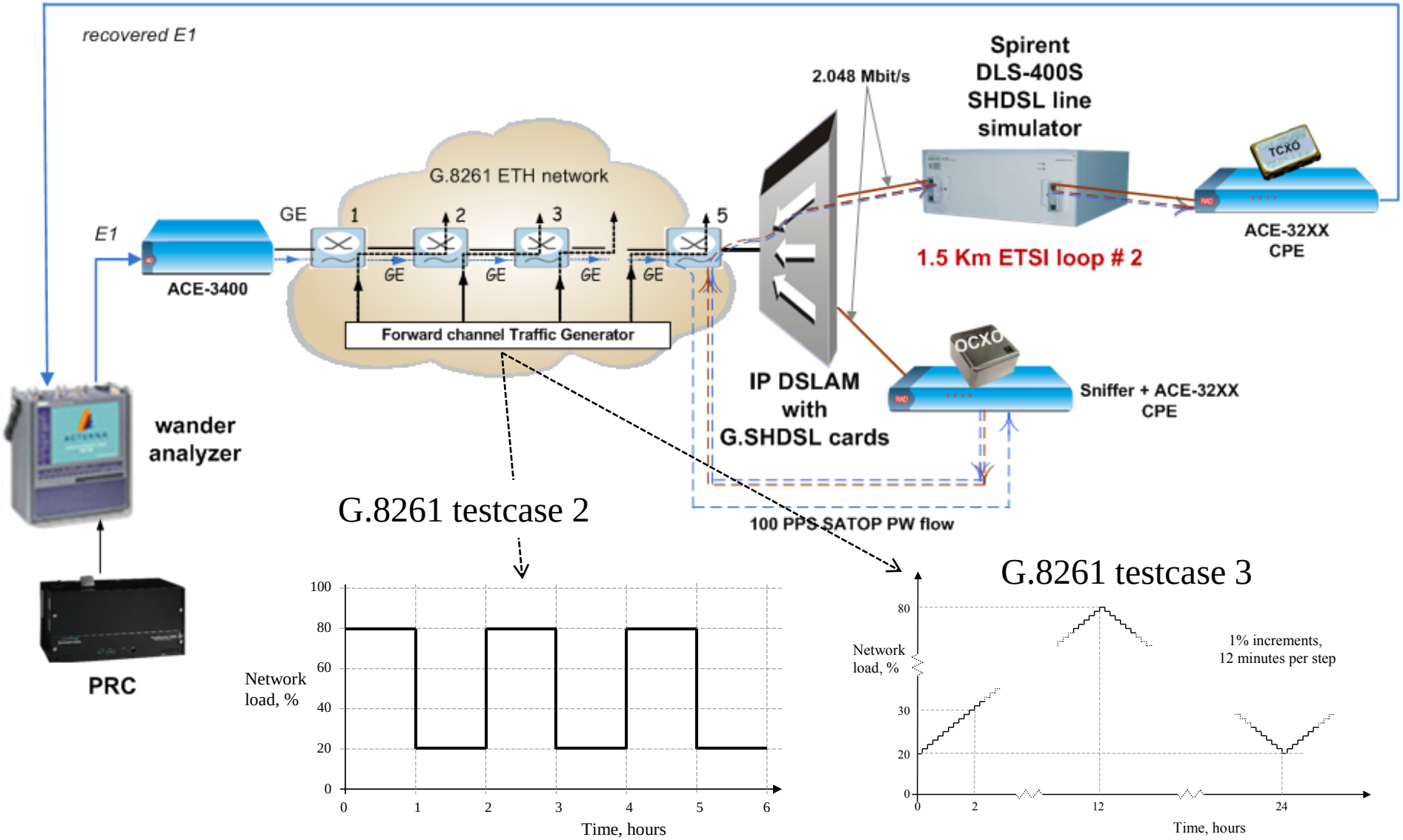


Examples of DSL 'sniffers' (III)



- Used when the PRC clock is installed in a remote location to the DSLAM
- The DSL sniffer has 2 physical ports:
  1. DSL link input
  2. Network input/output interface (to Rx the PRC tracebale ToP flow and Tx the Differentialy encoded information)

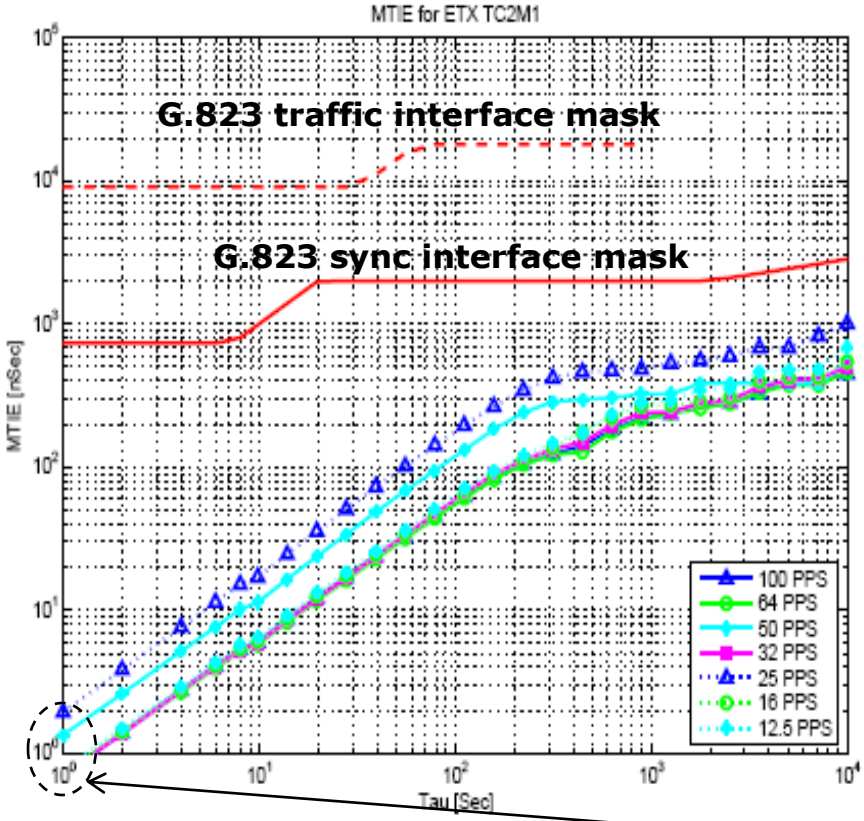
Clock distribution strategy III: real-world conditions lab test



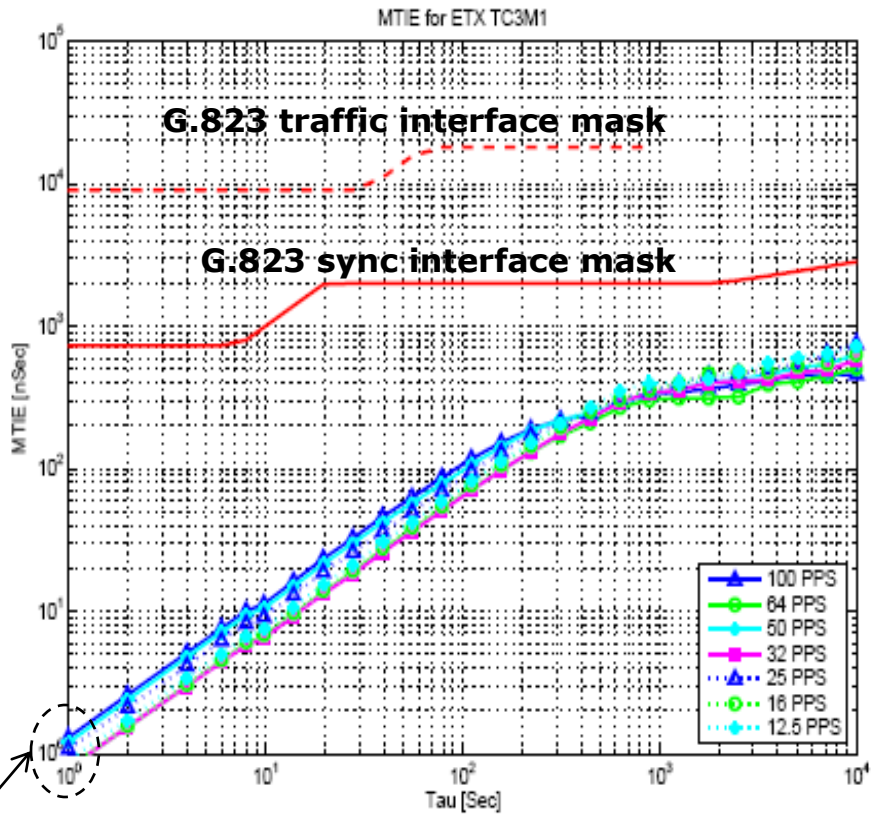
Clock distribution strategy II: clock recovery tests results (E2E)

Presented are the results for two G.8261 testing scenarios:

Test case 2
(20%-80% load alternations)



Test case 3
(24 hrs ramp-up test)



frequency accuracy ~1 ppb

What about TOD?

- In order to distribute TOD over DSL, one must measure the link delay on both directions (upstream and downstream)
- BUT, DSL services (especially asymmetric ones) tend to introduce inherit large asymmetry on the higher layers data propagation delay
- Hence, the problem must be solved by adding functionality to the physical layer
- ITU-T AG15/Q13 had decided, in the last meeting in Rome, to start working on that with the direct involvement of Q4 (DSL).

THANK YOU

Questions?