Building Adaptable Timing Synchronization Algorithms

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Topics

- **Challenges in Timing over Packet Networks**
- **FPGA Technology enabling Adaptable Timing Algorithms**
- **Usage Models**
  - Generic IEEE1588 Solution
  - Timing in Ethernet Switches
- **FPGA Clock Resources & Applications**
  - Full Digital Clock Synthesis
  - Phase/ Frequency difference measurements
- **Conclusions**

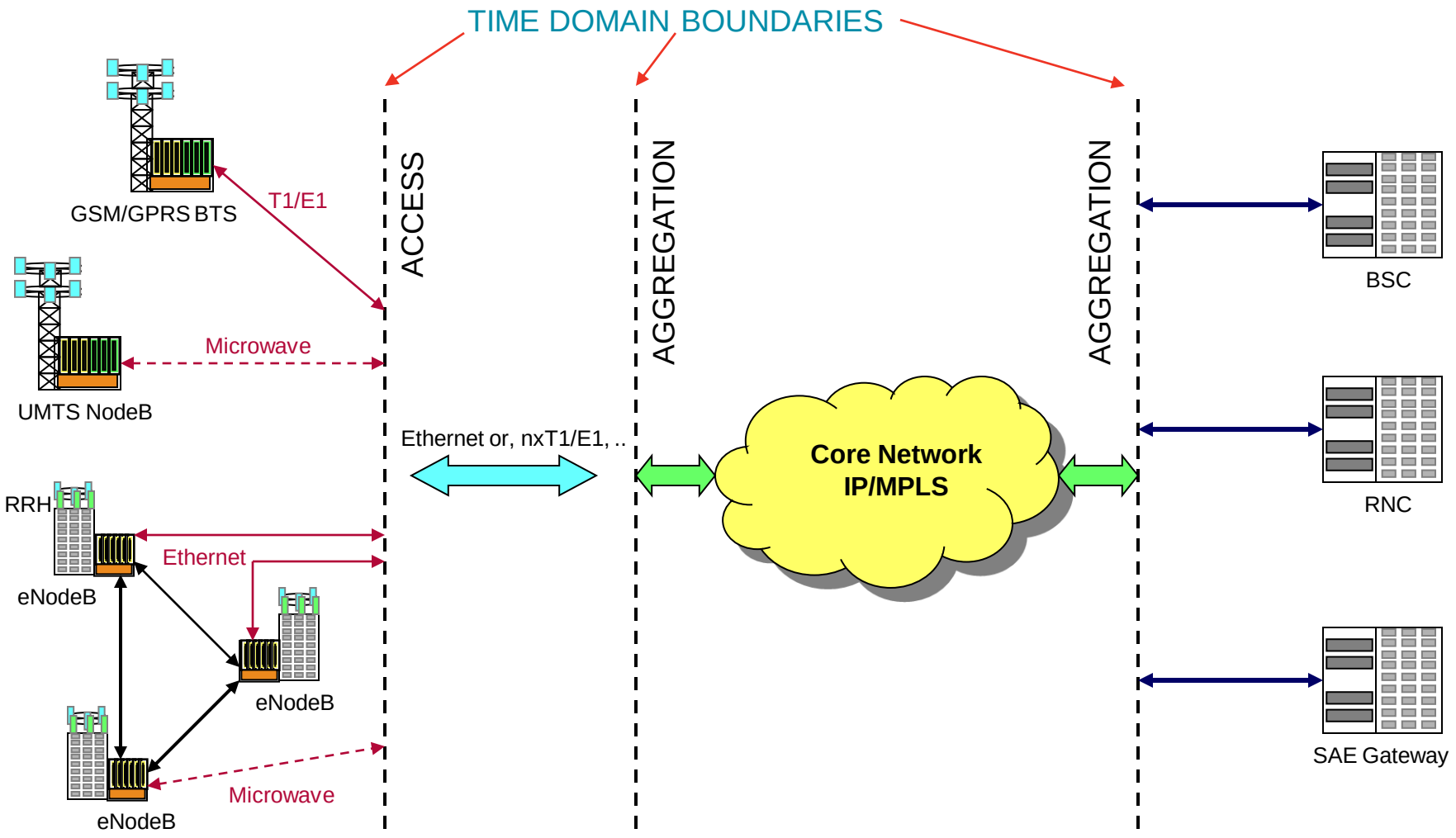
Timing Synchronization over Packet Networks

Challenges

- **Heterogeneous Networks:**
  - Gradual transition to IP based transport networks
  - Traditional TDM networks to co-exist for long time
  - No single timing protocol adequate to address timing requirements
  - Varying timing synchronization requirements (time/ freq, phase)
- **IEEE1588 PTP**
  - Susceptible to network imperfections and packet delay variations
  - Proprietary algorithms needed to filter out network imperfections
  - Exposed to network security issues
  - Requires expensive oscillators to achieve carrier grade accuracy
- **Synchronous Ethernet**
  - Difficult to achieve end to end SyncE connectivity
  - Delivers only frequency synchronization

Timing Synchronization Flow

Wireless Infrastructure Network



Time accuracies tend to degrade across time domain boundaries

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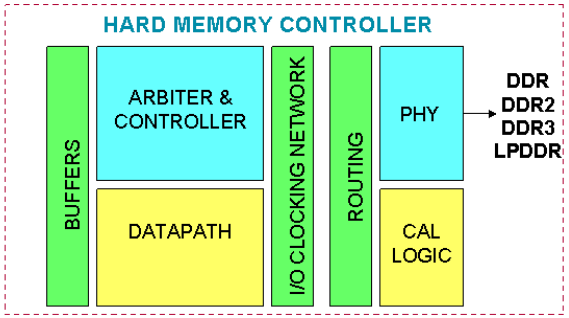
Addressing timing over packet challenges

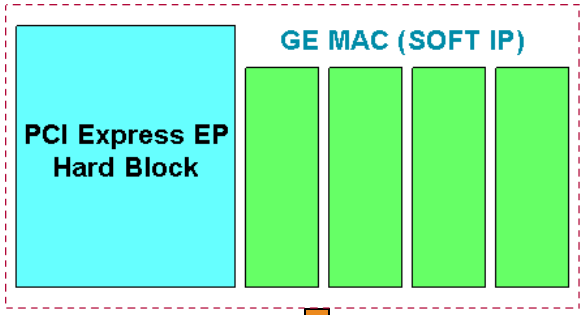
FPGA a significant play

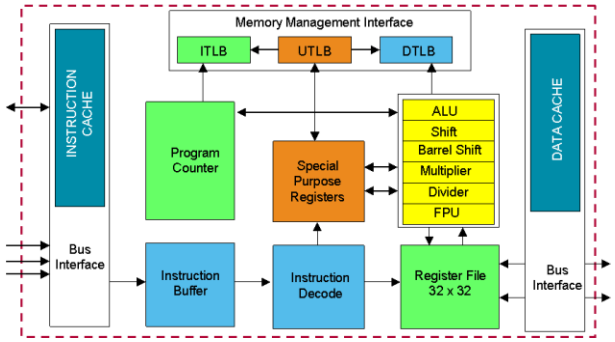
- **Incorporating OAM in networks to overcome impairments**
  - Ethernet switches using OAM (802.3ah, 802.1ag, ITU Y.1731)
  - MPLS forum working on OAM definition along similar lines
- **Approaches to improve timing accuracy**
  - Use multiple timing protocols for correlation & accuracy improvement (SyncE + IEEE1588 wherever possible)
  - Digital & statistical algorithms to filter network delays & asymmetry
  - Implementing transparent clock at switch ports
- **FPGA devices positioned to play a significant role**
  - Attractive platform to build a flexible & adaptable timing solution
  - Multiple vendors supporting IEEE1588 on FPGA
  - Synchronous Ethernet support as part of on chip SerDes
  - Significant presence in Ethernet Switching & MPLS packet classification

Low Cost FPGA

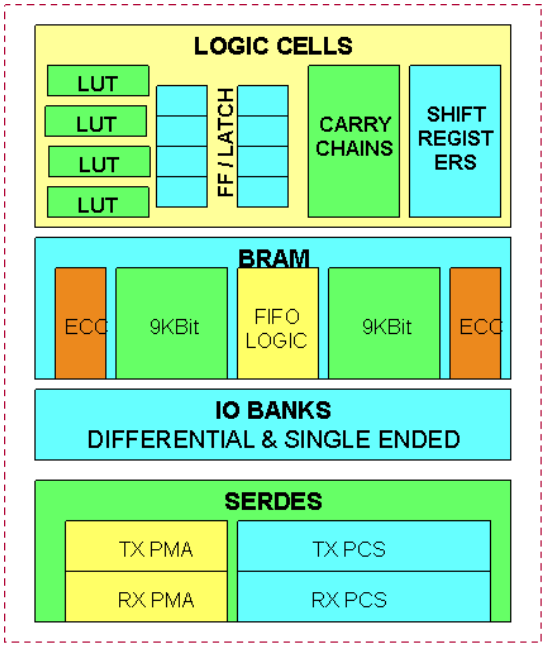
Xilinx Spartan-6 FPGA Architecture

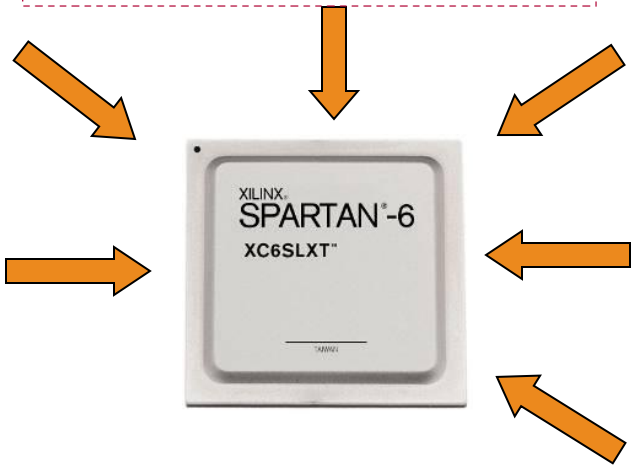


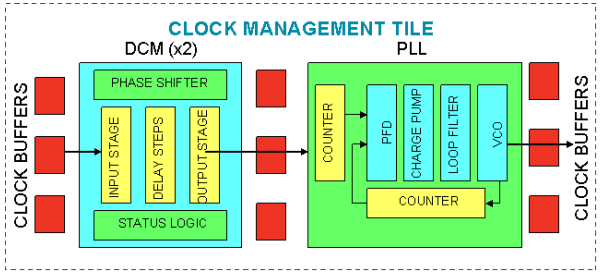


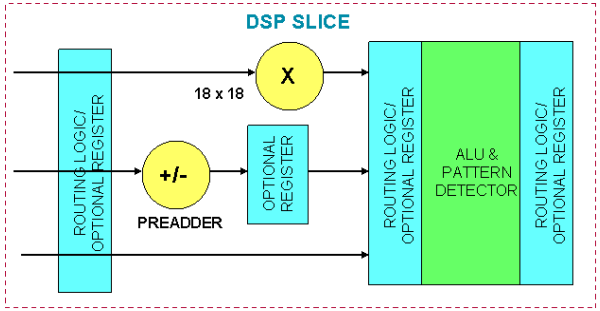


Microblaze soft processor









Low Cost and high performance Xilinx Spartan-6 in 45nm low power process technology

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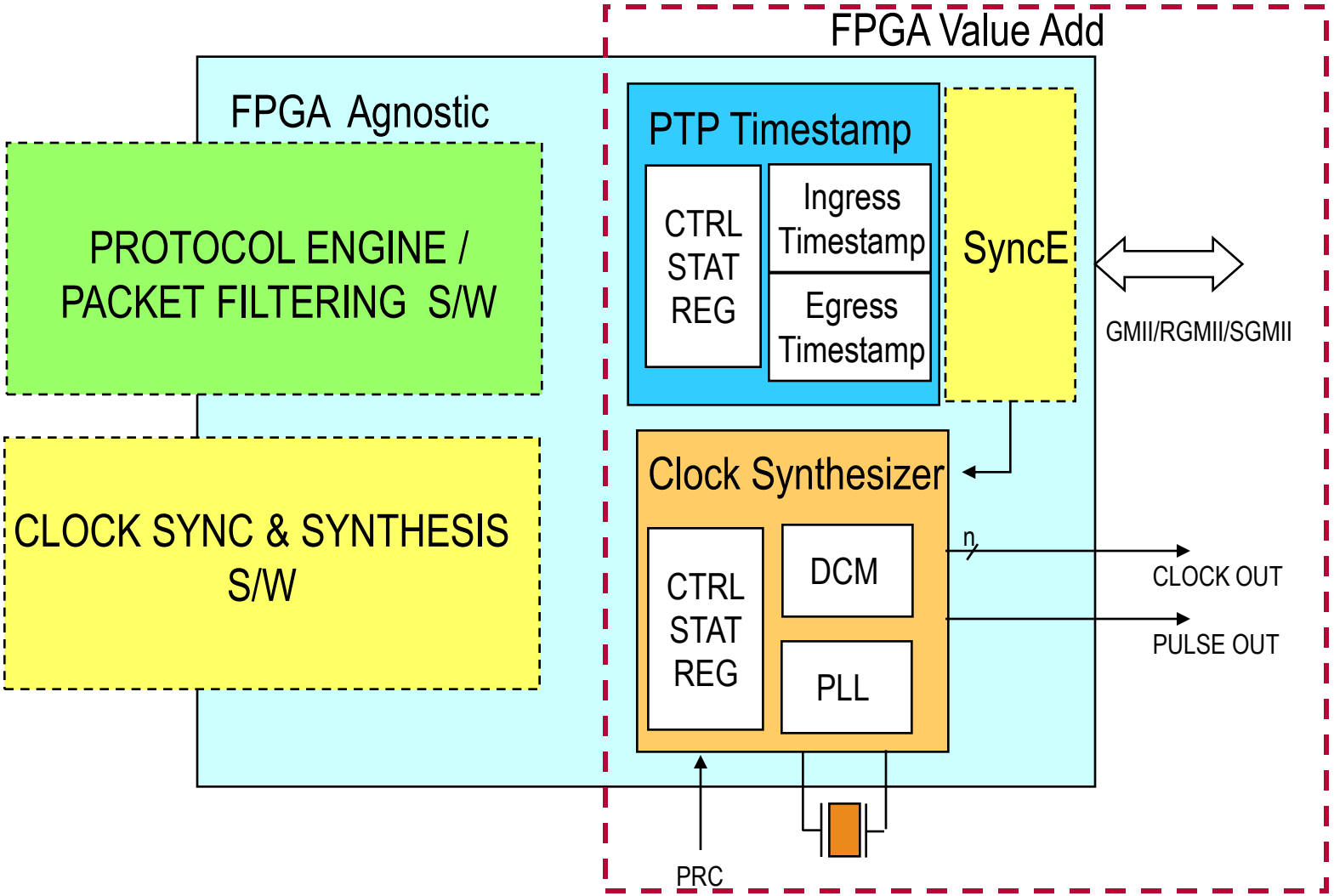
Generic Timing Solution

Ordinary Clock Implementation



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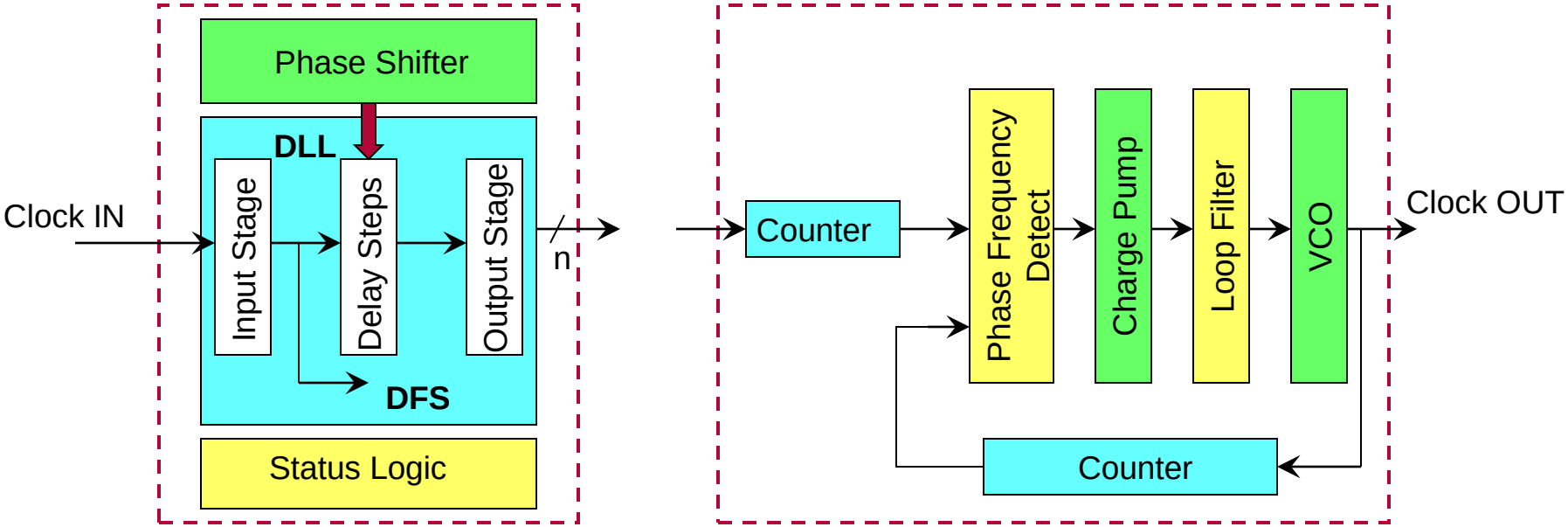
FPGA Clock Resources

Digital Clock Managers & PLL



Digital Clock Manager & PLL

DLL – Delay Locked Loop
DFS – Digital Frequency Synthesis

- Enables use of free Running Oscillator
- Eliminates Clock Skew
- Phase shift input clock by fixed or fraction

- Synthesize new frequency by dynamic clock multiplication and division
- Clock Input Jitter Filtering/ re-buffer
- Spread Spectrum Clock Generation

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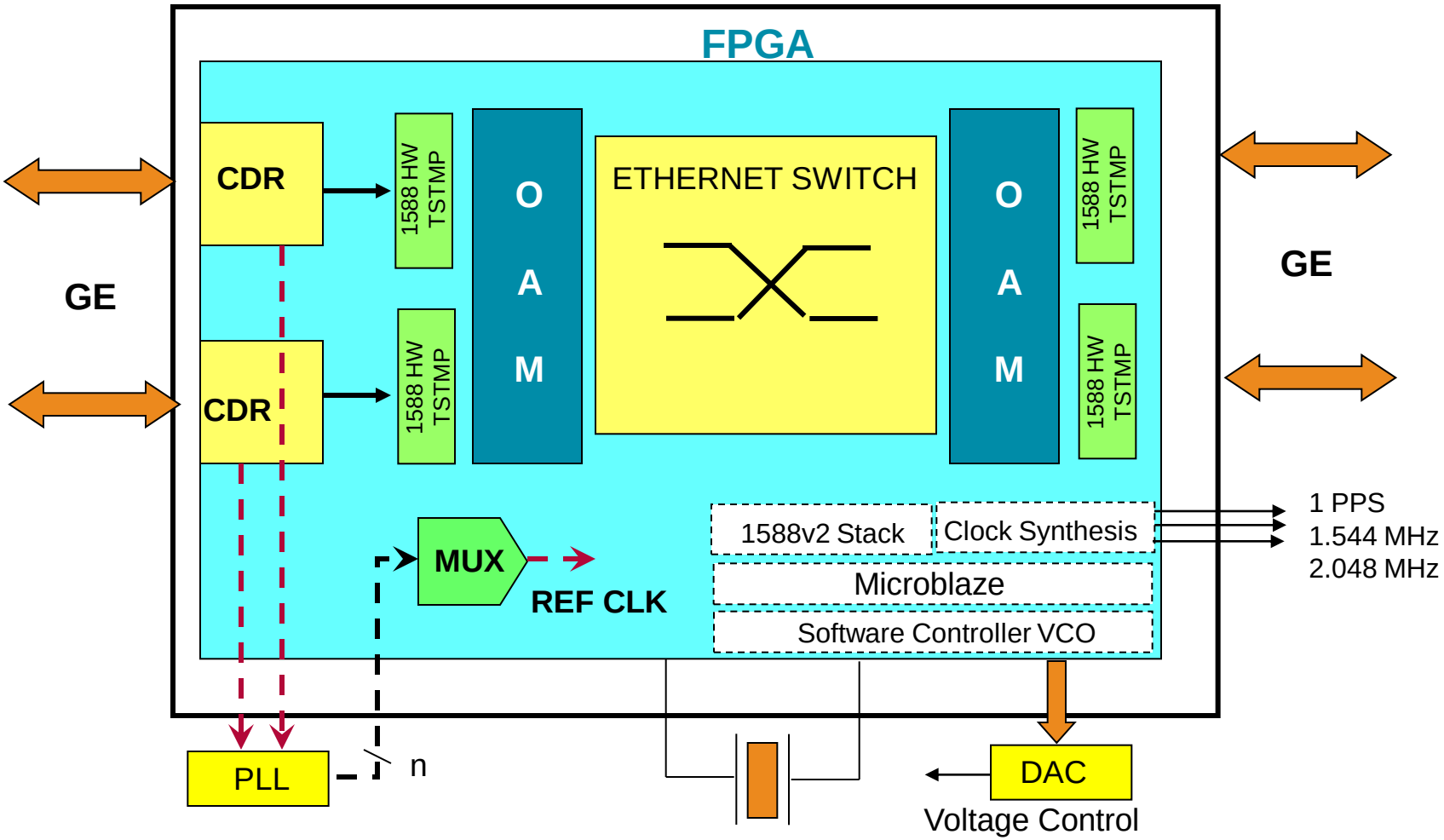
Timing IP in Packet Networks

Full Digital Clock Synthesis



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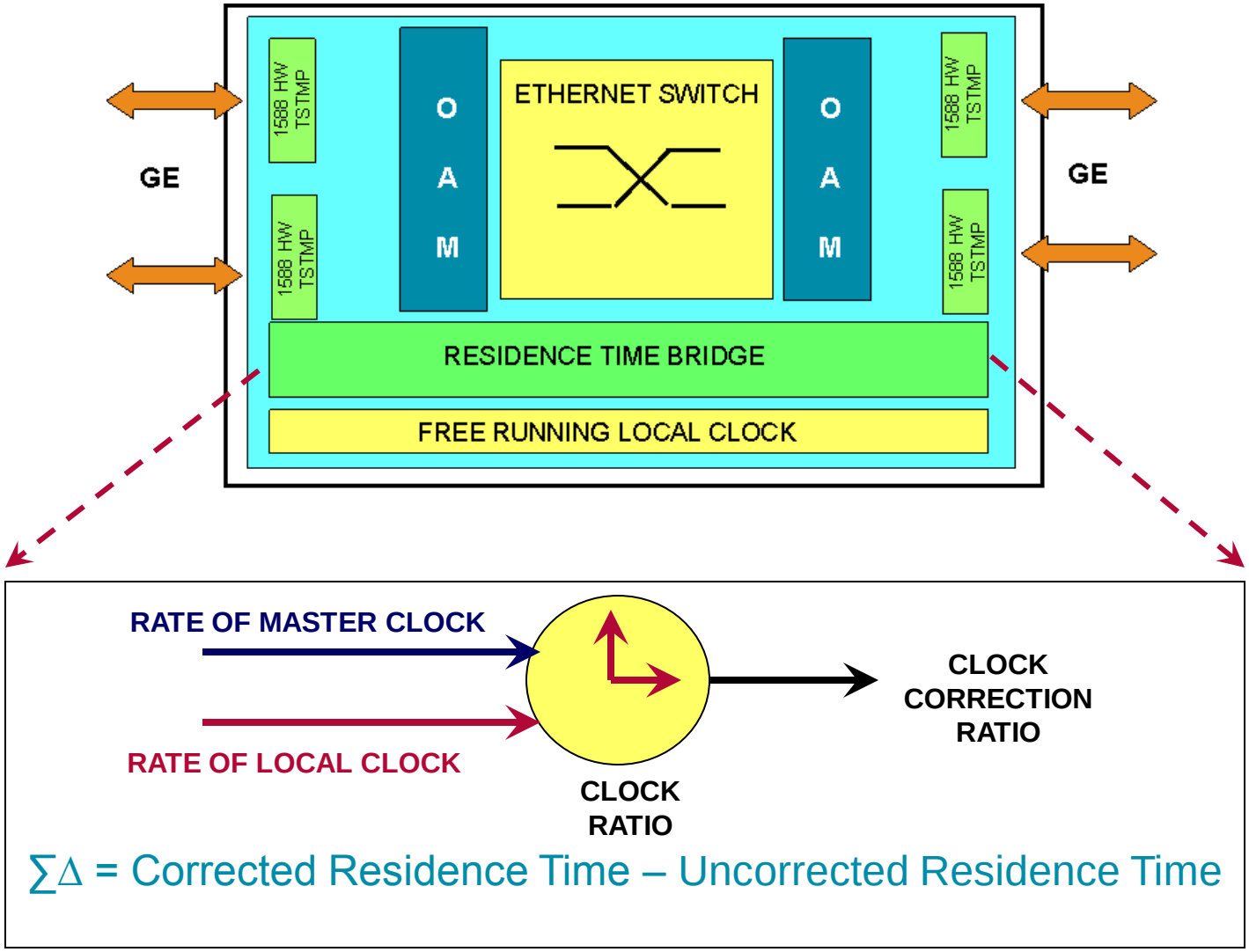
Transparent Clock – Residence time bridge

Phase/ Frequency Difference Correction



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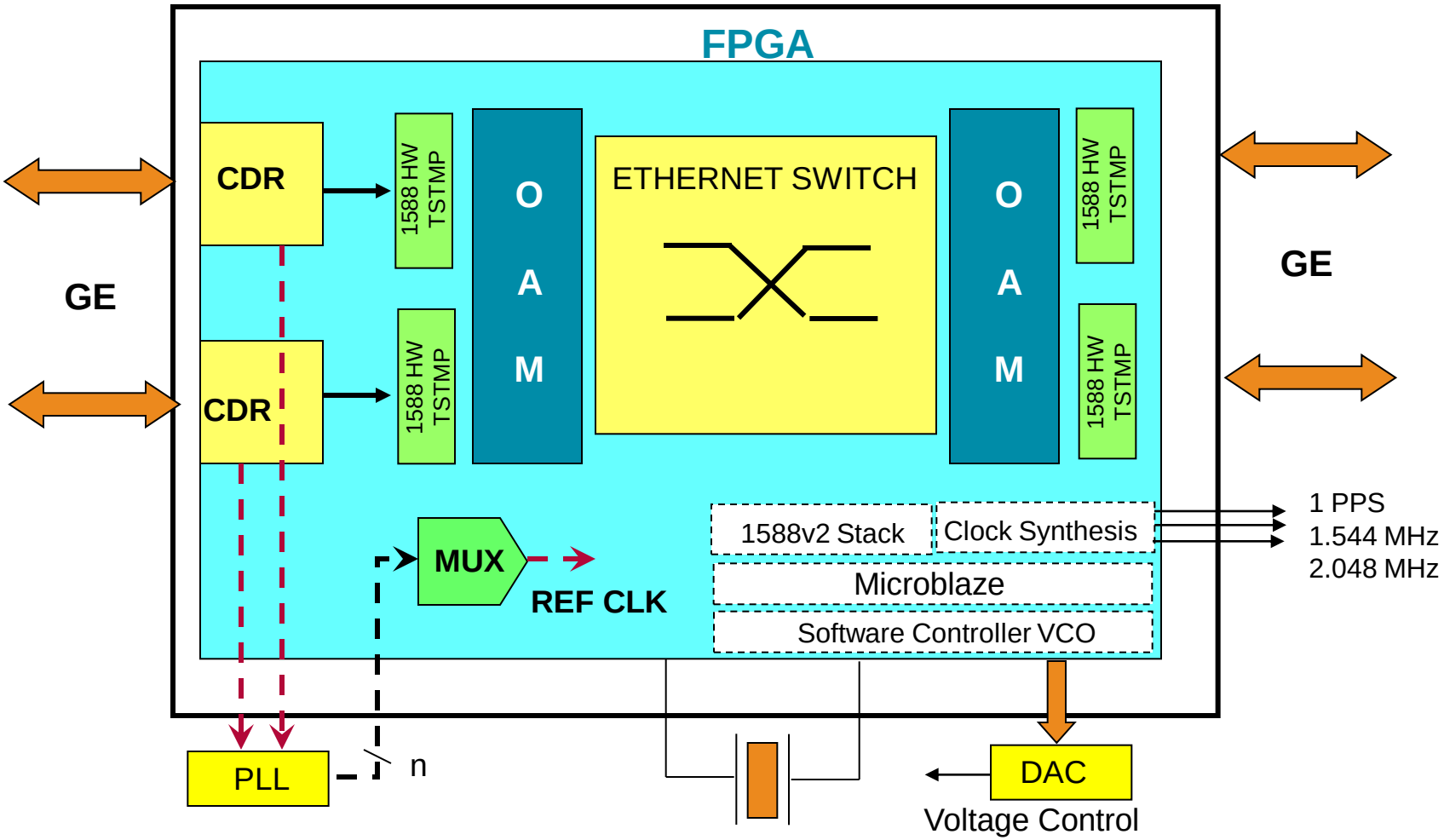
Timing IP in Packet Networks

Full Digital Clock Synthesis



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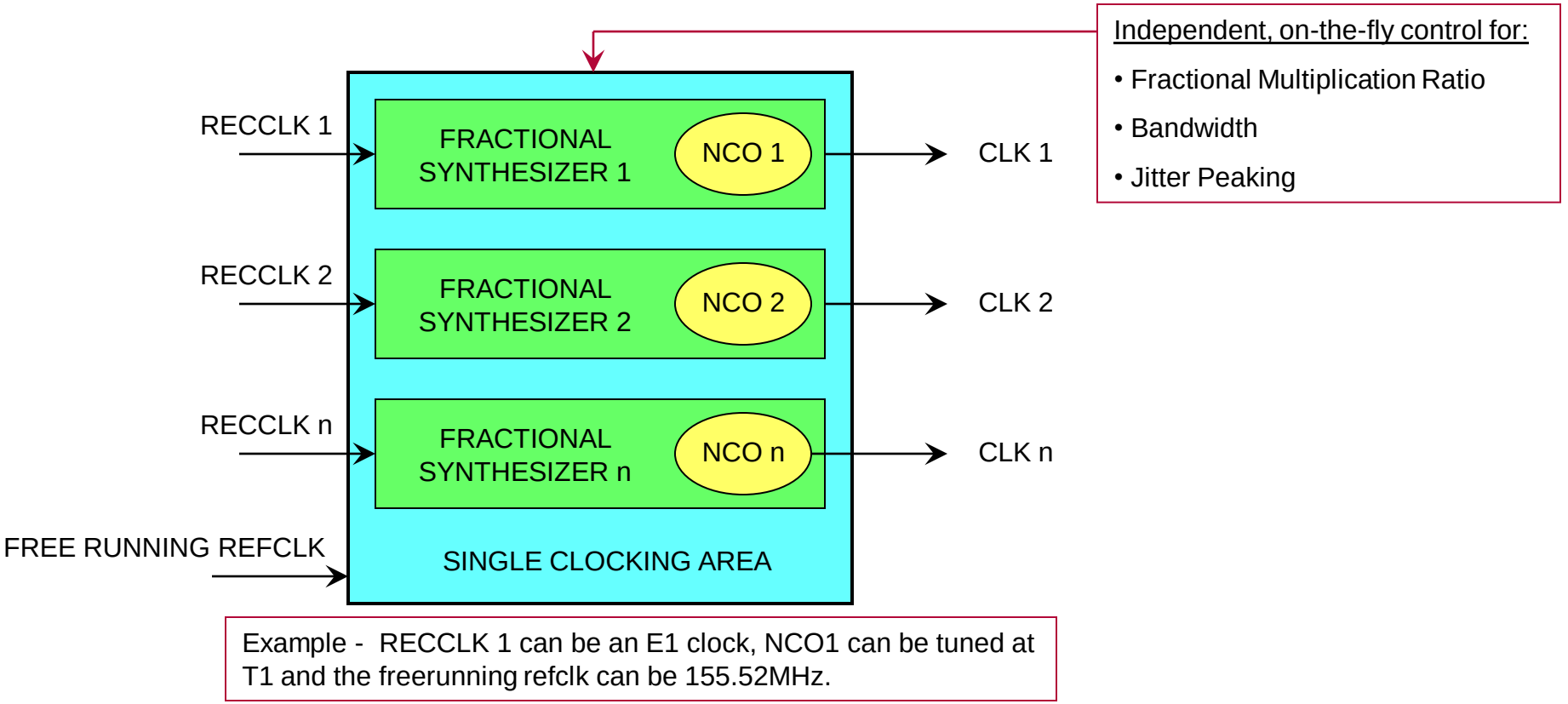

- Fully synchronous structure.
- Dynamic reconfiguration of frequency, bandwidth and jitter peaking.
- Low Cost Solution - No DAC, External VCO, or Analog Loop.

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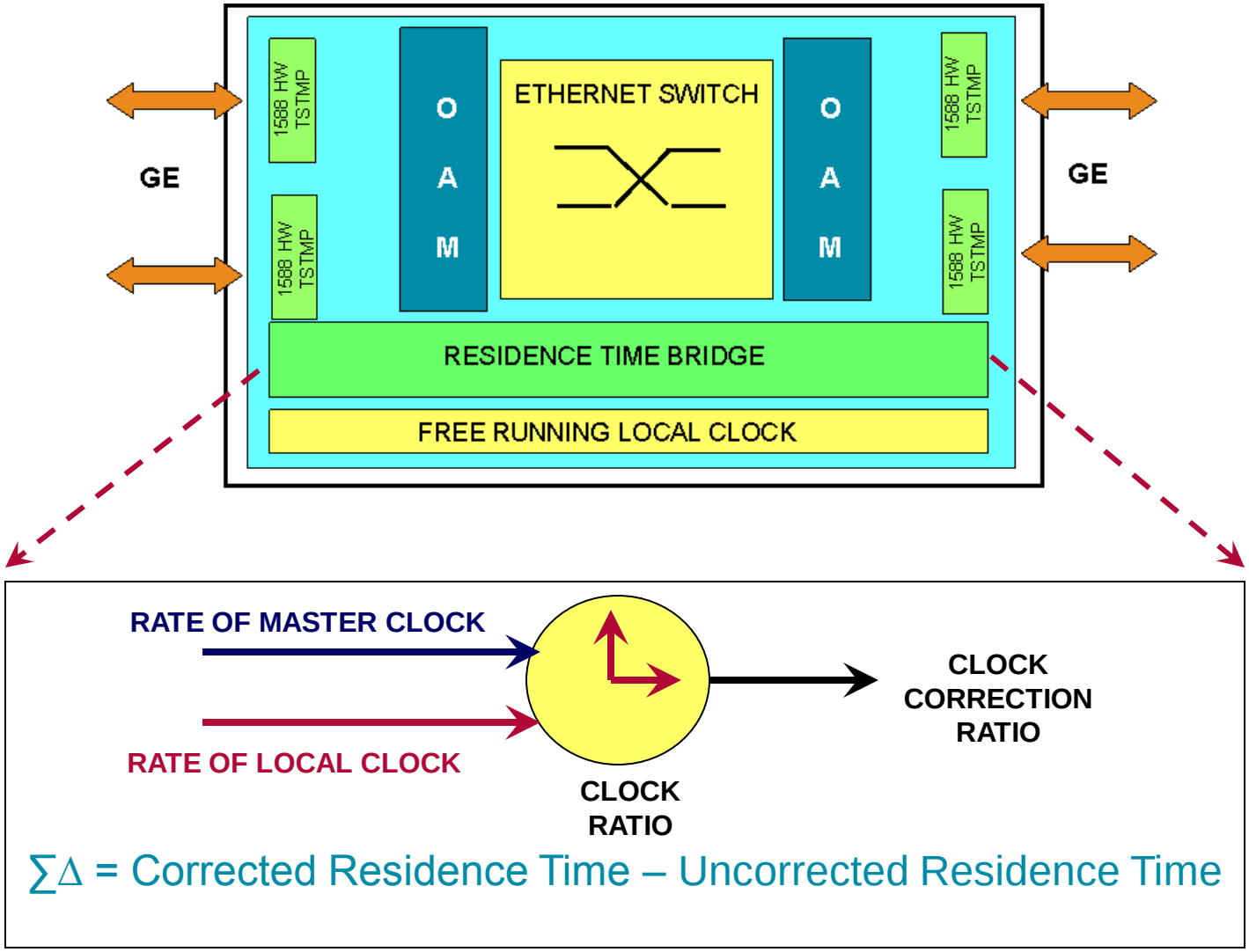
Transparent Clock – Residence time bridge

Phase/ Frequency Difference Correction



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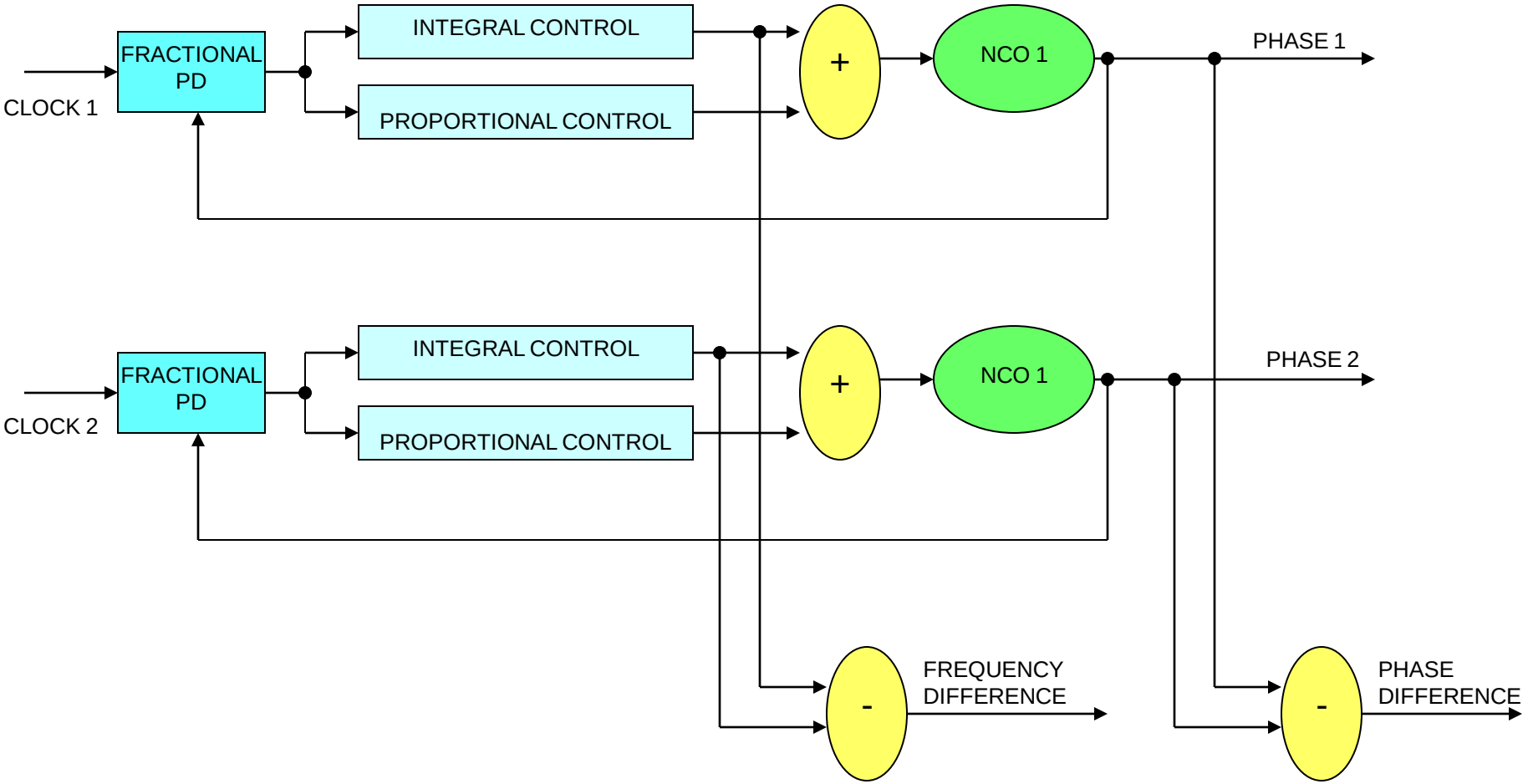
Phase/Frequency Difference Measurement



The single clock area allows for easy real-time monitoring of frequency and phase difference between 2 clocks.

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Conclusions

- **Challenges in implementing Timing over Packets**
  - Heterogeneous Networks
  - Co-existence of legacy equipment
  - Varied Network imperfections
- **Adaptable Timing Algorithms needed**
  - Application specific Timing accuracy requirements
  - Standards based timing algorithms for widespread deployments
  - Proprietary algorithms needed on top of standards based protocols to correct network imperfections and allow cost versus timing accuracy tradeoff
- **FPGA Technology enables adaptable Timing Algorithms**
  - Ease of implementation flexible & adaptable timing solutions
  - Excellent platform to host proprietary algorithms
  - On chip SerDes clock data recovery circuit for SyncE
  - Full digital clock synthesis, measurement, and correction