Network Timing Reference for Frequency Synchronization in xDSL based Access Networks

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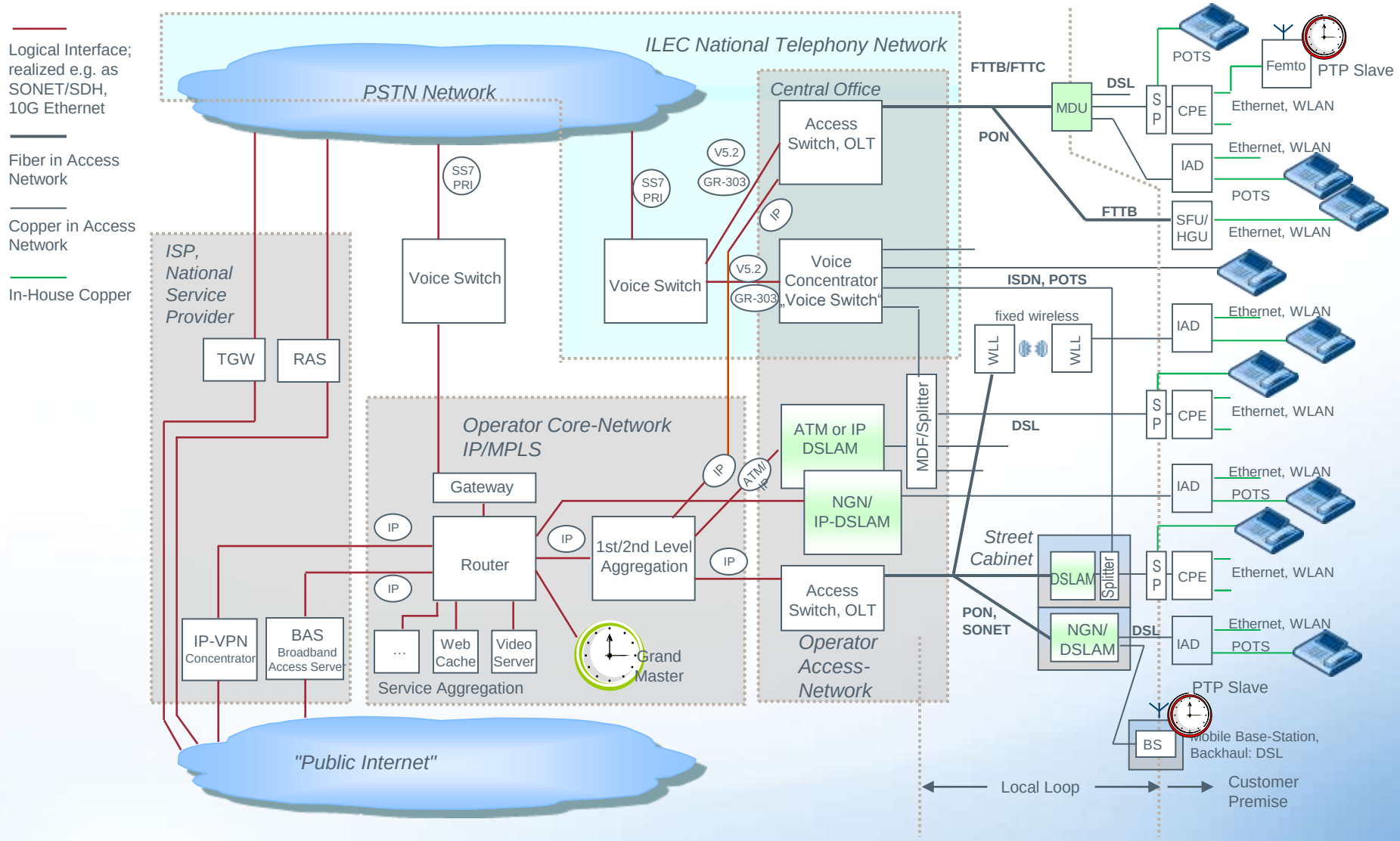
Frequency & Time Distribution in xDSL End-to-End Networks



History and Future of Clock Synchronization over DSL

As of today…

- ADSL, VDSL for data services, residential customers
  - no requirements for frequency & time synchronization
- SHDSL mostly for business (symmetrical) data-services
  - Rather limited use for frequency synchronization
- Backhaul of Base-Stations over copper addressed with T1/E1
  - high precision frequency & clock distribution through TDM framing with native baud-rate (2.048MHz, 1.536MHz)

Future:

- Mobile evolution demands frequency synchronization till the edge of the access network
  - Pico/Femto-Cell architectures for mobile networks, operated in customer's premise
  - Bandwidth demand, exceeding T1/E1 capacity
  - Backhaul of 3G/4G Base-Stations partially through (bonded-) DSL

xDSL Technology Overview

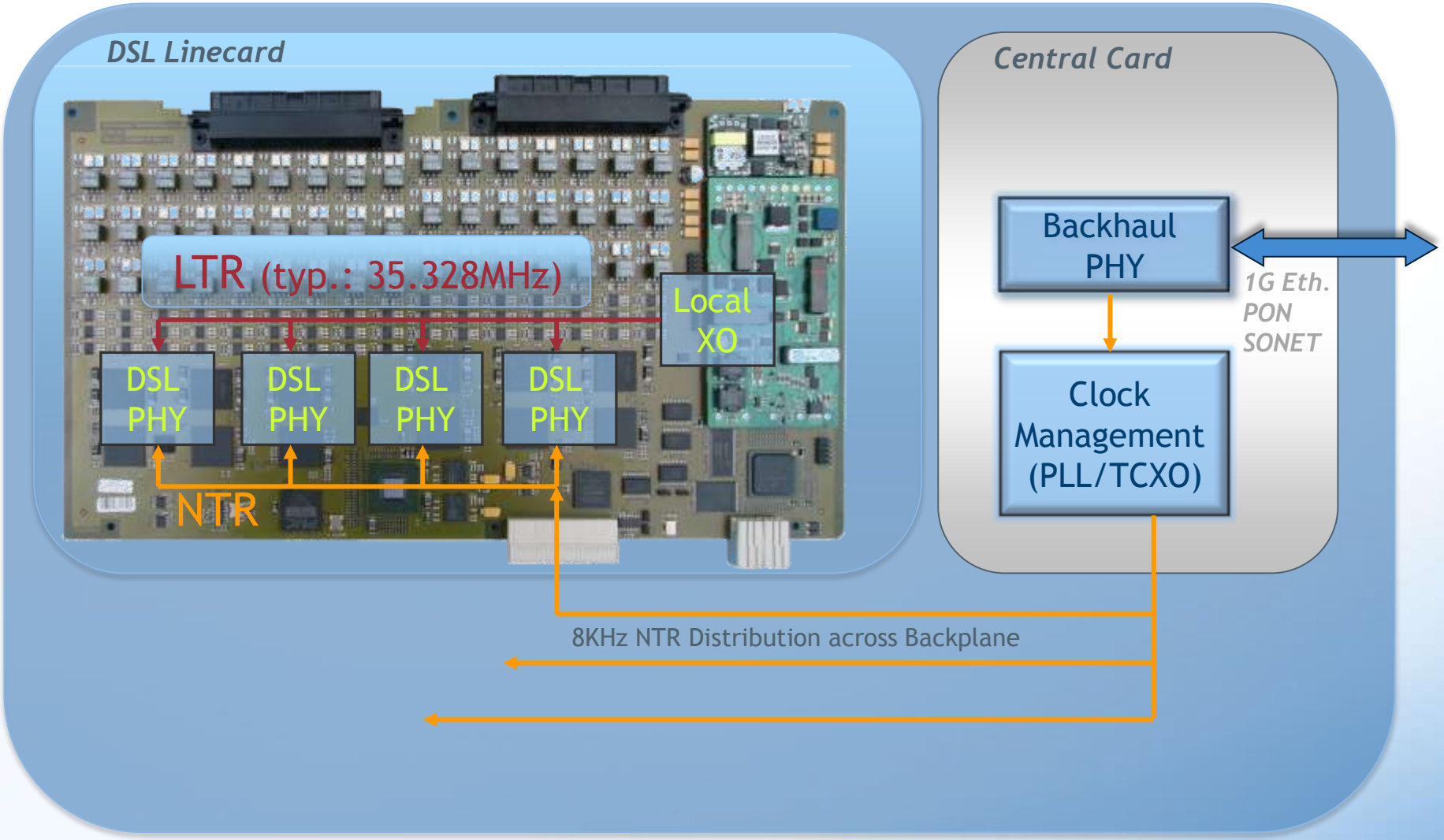
	 SHDSL	 ADSL2+	 VDSL2
DS data rate	5.7 Mbps	28Mbps	100 Mbps
US data rate	5.7 Mbps	1~3 Mbps	100 Mbps
Typ. loop length	24 kft	12...20 kft	6...10 kft
Layer 2 Transp.	PTM, ATM,TDM	ATM, PTM	PTM, (ATM)
Typ. Deployment	Ex	Ex, Cab	Ex, Cab, Bld.
Max. Signal BW	1.4 MHz	2.2 MHz	30 MHz
Modulation	PAM 16/32	DMT 512 /32 carriers	DMT 4096/4096 carriers
Transmit Power	14.5 dBm	20.5 dBm	14.5, 20.5 dBm
Frequency Sync	NTR sync	NTR inband,sync	NTR inband, sync

Time and Clock Syncronisation for DSL – Overview

	Legacy DSL NTR	Future (Proposed) Time-of-Day Transmission Convergence Layer for DSL
Reference	G.991.2 (SHDSL) G.992.1 (ADSL) G.992.3, G.992.5 (ADSL2, ADSL2+) G.993.2 (VDSL2)	ITU-T Contribution 10MB-054R1 (and others) for VDSL2
Maturity	available/mature	basic idea; principle based on IEEE1588
Frequency Sync	Yes	Yes
Phase Sync	---	Yes
Abs. Time Sync	---	Yes
Working Principle	NTR ib-bits (indicator bits), exchanged every superframe (≤20ms)	1588 PTP-style exchange of 4 timestamps; time events coupled to DSL-loop timing

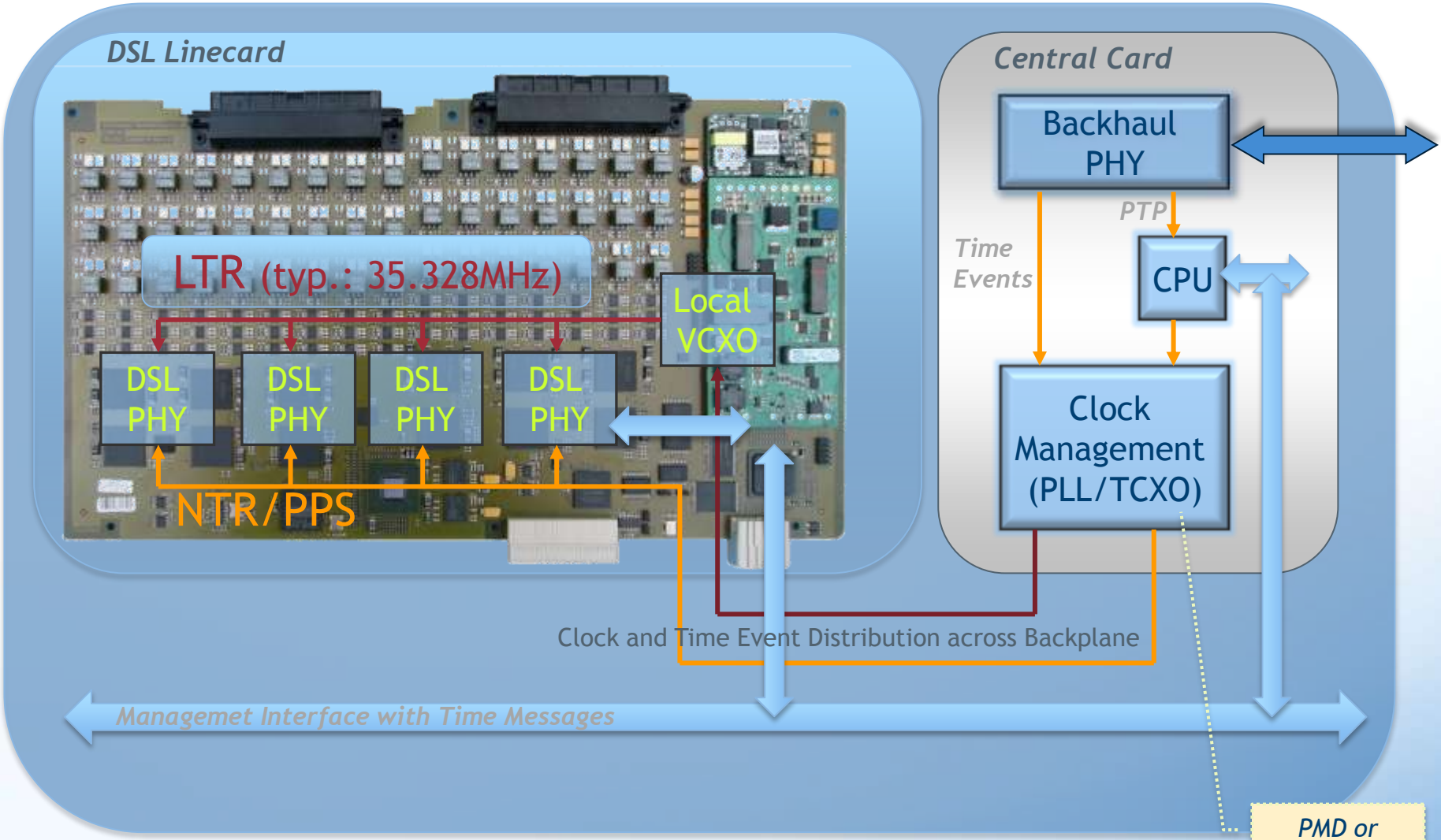
Clock & Time in a DSL DSLAM - LTR and NTR

Generic View of Today's Systems (Simplified)



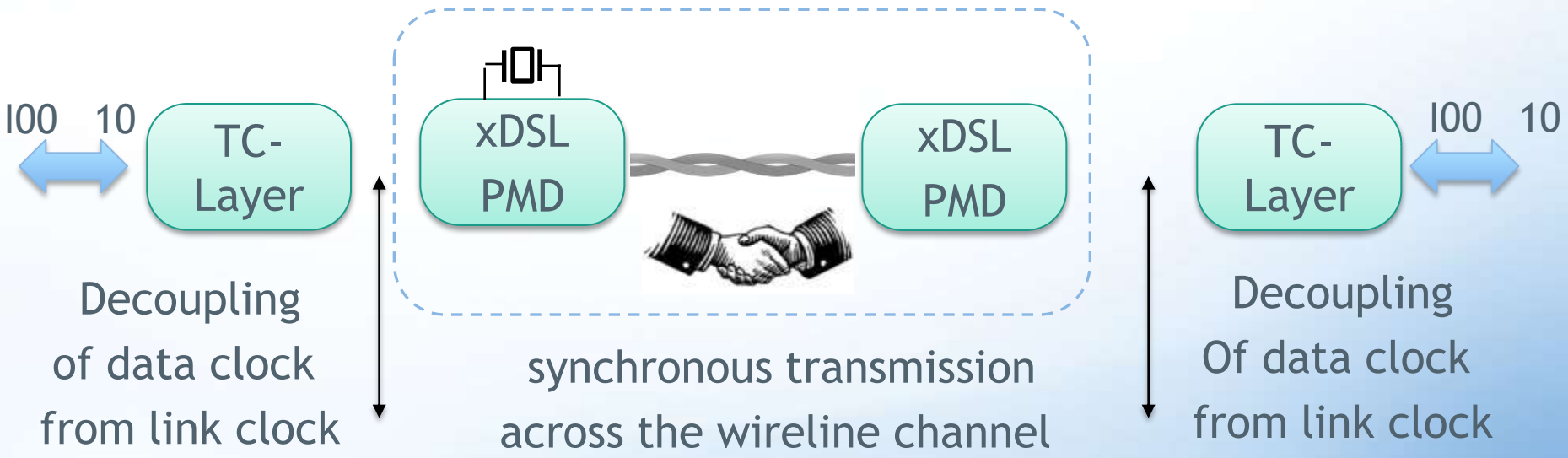
Clock & Time in a DSLAM - Advanced Architectures

Generic View (Simplified)

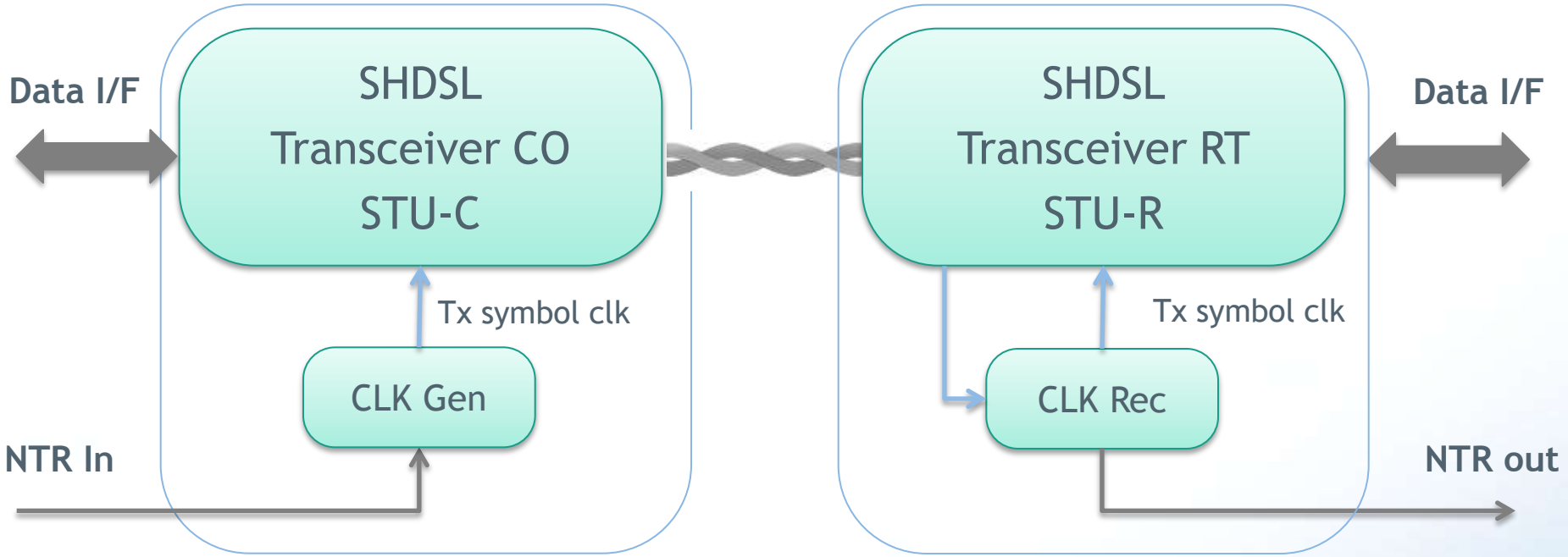


Working Principle of NTR:
Frequency Synchronization across xDSL Links

- The well known xDSL technologies ADSL, VDSL and SHDSL include Transmission Convergence Layers which decouple data streams timing from transmission timing due to its focus on ATM or PTM framed data
- In order to support frequency synchronization across the xDSL link the xDSL standards define methods to transport a Network Timing Reference (NTR) across the DSL link



Network Timing Reference for Frequency Synchronization – SHDSL

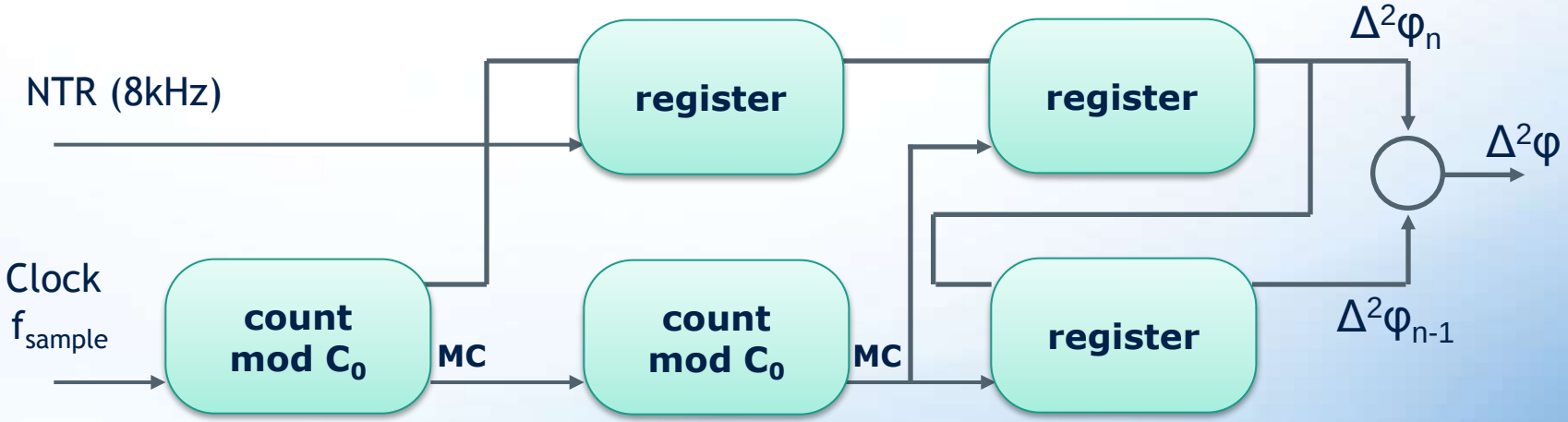


- SHDSL supports Network Timing Reference from STU-C to STU-R
- In NTR mode frame and symbol clock are locked to the NTR time marker (8kHz or a multiple thereof, e.g. 1544 kHz or 2048 kHz,)
- At the STU-R the NTR is extracted from the recovered Frame or symbol and provided to the data layer

NTR – In-band Transport

- NTR and xDSL clock need not be synchronous
- NTR information is transported by differential phase offset values between the NTR and the Local Timing Reference (LTR)
- The LTR is derived by dividing the ADSL / VDSL2 sampling clock by the xDSL flavor specific factor
- The phase offset is expressed in cycles of the sampling clock at Nyquist rate as a 2-complement number

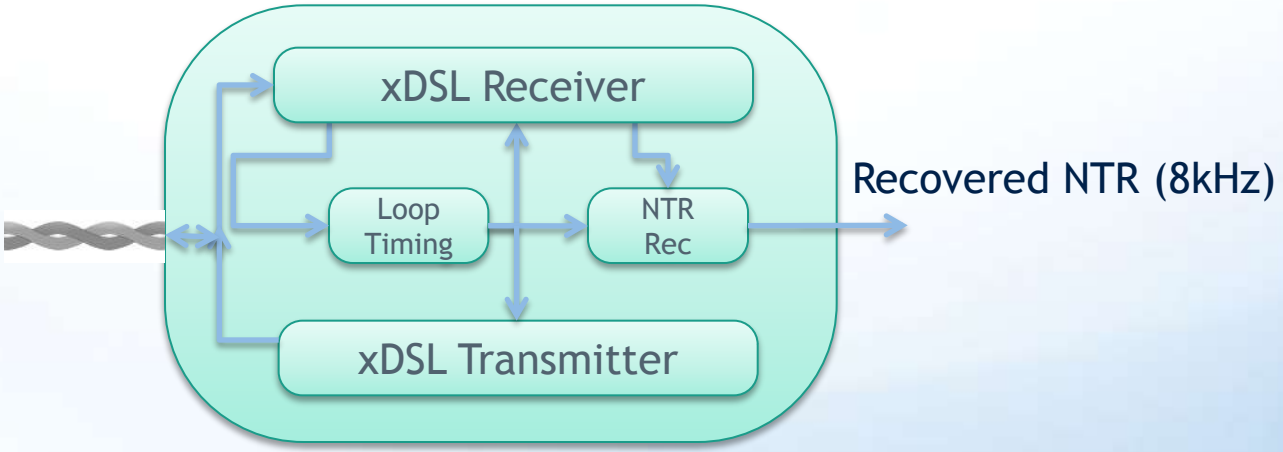
Generic Architecture



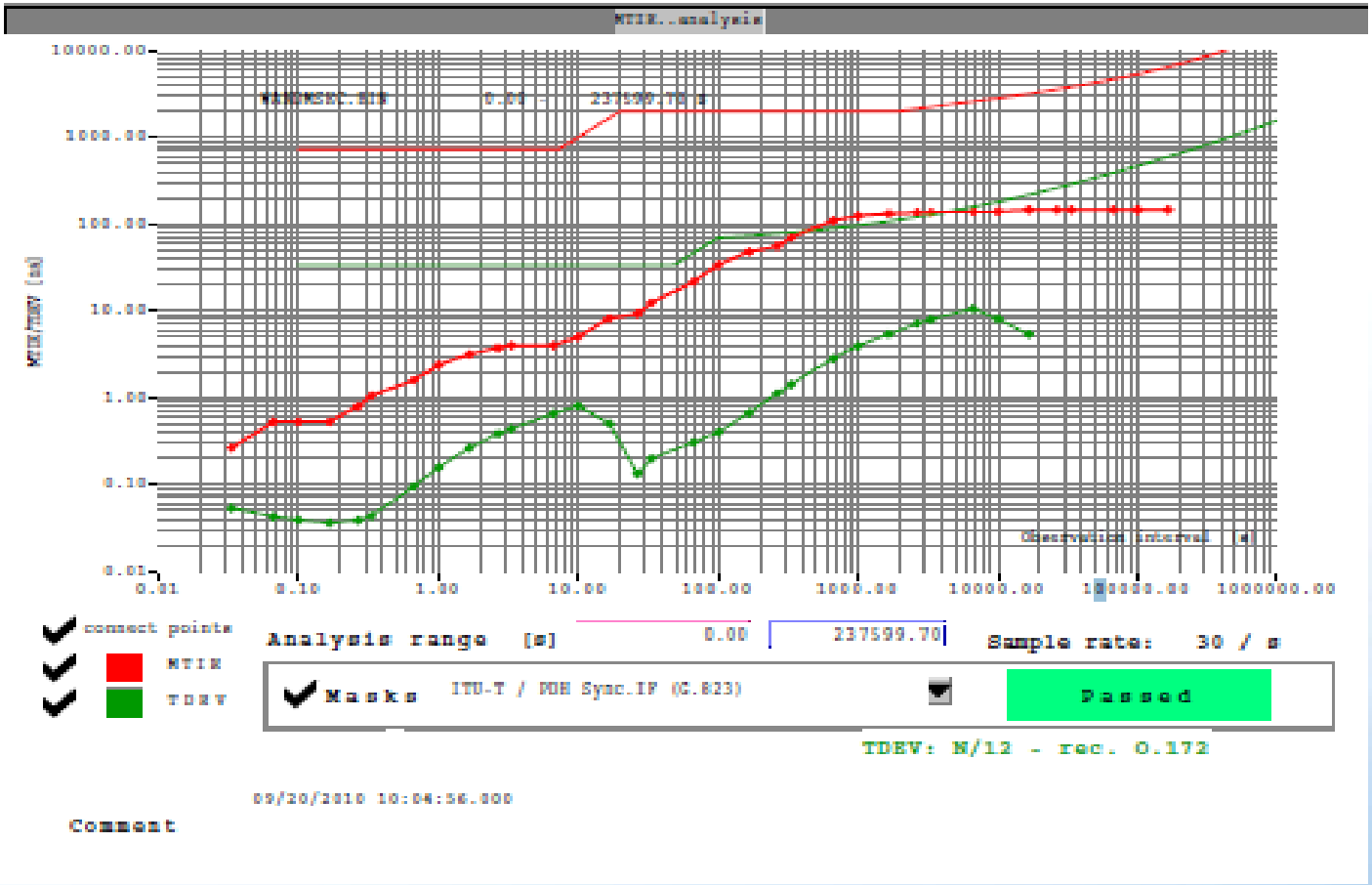
Network Timing Reference for Frequency Synchronization – ADSL, VDSL2 - NTR – In-band Transport

Properties

- NTR information is transmitted with every Overhead Channel Period of the actual DSL link, i.e.
  - 15-20ms in ADSL2+
  - < 20ms for VDSL2
- NTR updates are protected by CRC check sum
- Intermittent outages do not result in accumulating errors
- At CPE side NTR is recovered based on recovered loop timing and received NTR information



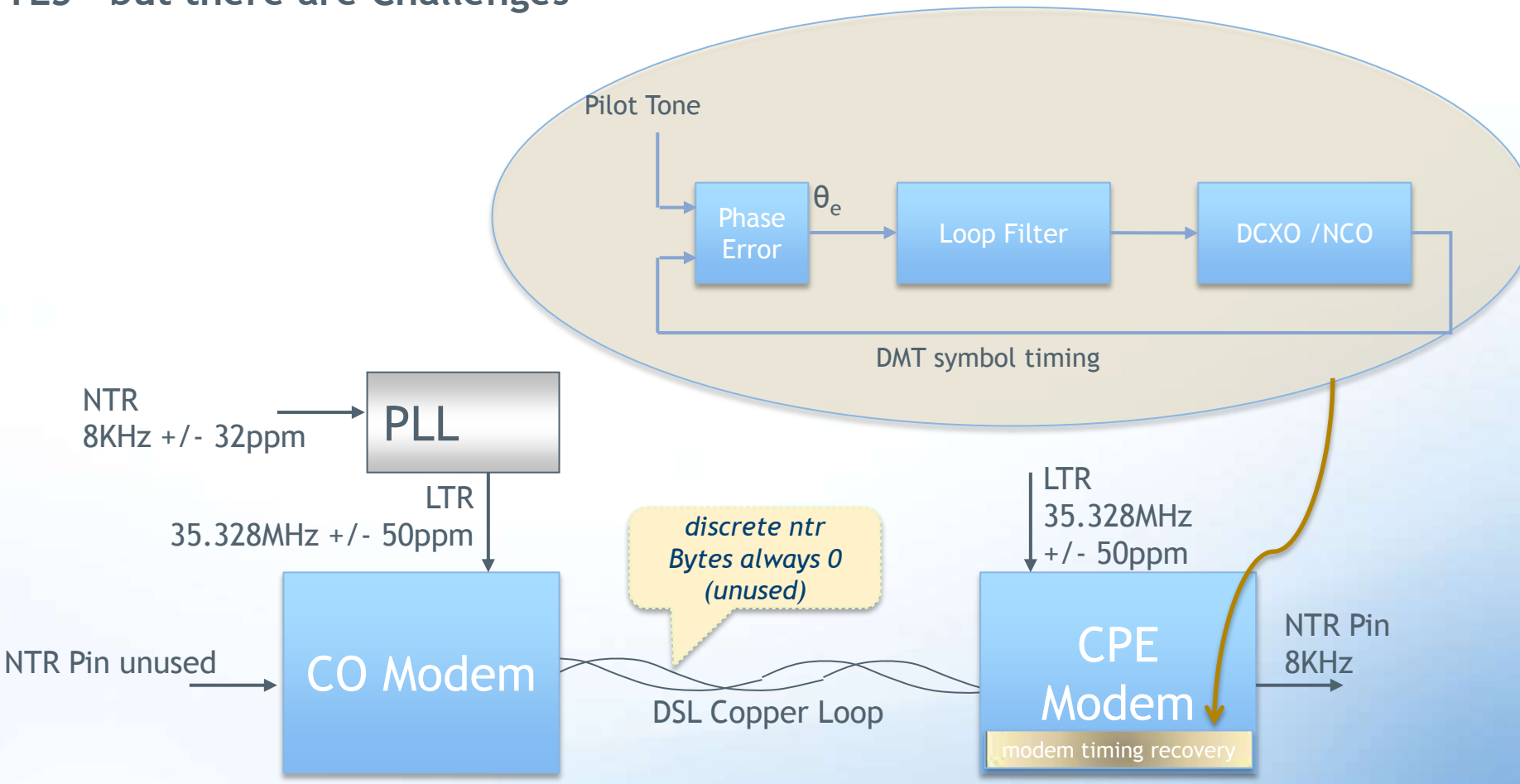
- MTIE / TDEV Measurement:
  - NTR across a VDSL2 link



Network Timing Reference for Frequency Synchronization –
ADSL, VDSL2 - NTR synchronous to loop timing ?

Is it possible to have the VDSL2 loop timing synchronized to the NTR clock ?

YES – but there are Challenges



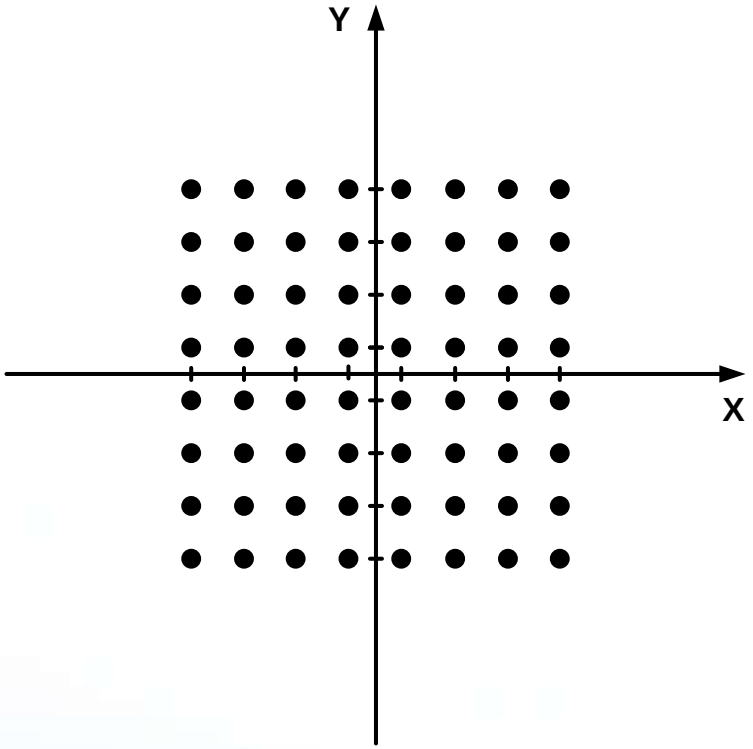
Network Timing Reference for Frequency Synchronization – ADSL, VDSL2 - NTR synchronous to loop timing ?

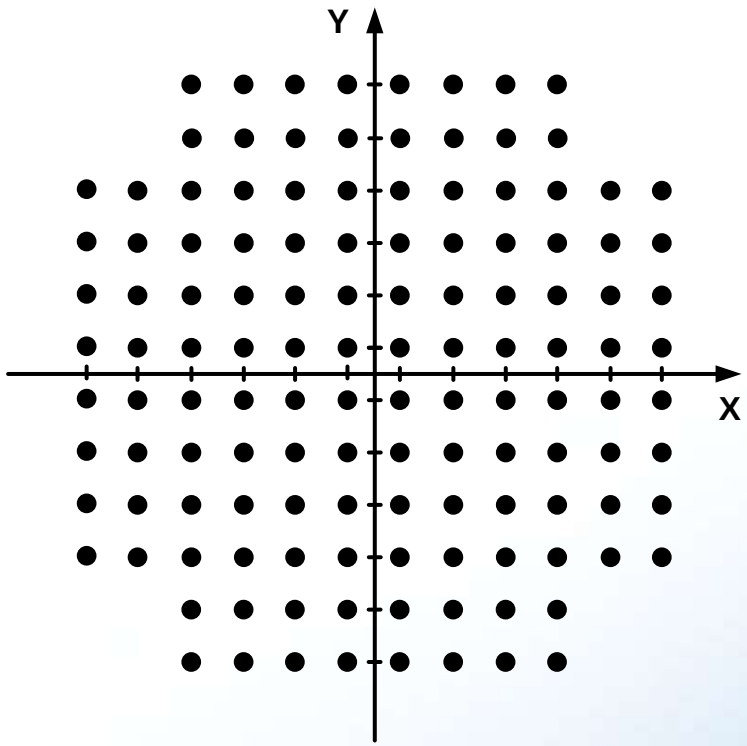
Implication of synchronous NTR transport with ADSL, VDSL2

- ADSL and VDSL2 utilize complex (dense) QAM constellations compared to legacy communication schemes
  ➔very low tolerance on clock jitter and wander for error free communication

- Clock requirements for xDSL systems are not specified in MTIE or TDEV tolerance schemes but in ppm frequency offset – not covering any jitter, wander or frequency drift limits
  - ➔ Potential interoperability issues with installed base as there is no specification on clock tolerances for xDSL implementations
  - ➔ DSLAMs require sophisticated clock regeneration techniques, if DSL LTR is to be synchronized with an NTR source
  - ➔ Holdover and fallback modes without phase jump needed to avoid link drops

Phase Jitter Impact on dense xDSL Constellation QAM Constellations per Carrier as per ADSL / VDSL2





- Square constellations for
- b=2,4,6,8,10,12,14 bits per symbol

➔4, …, 16384 constellation points.

➔Example: b=6, K=64 points

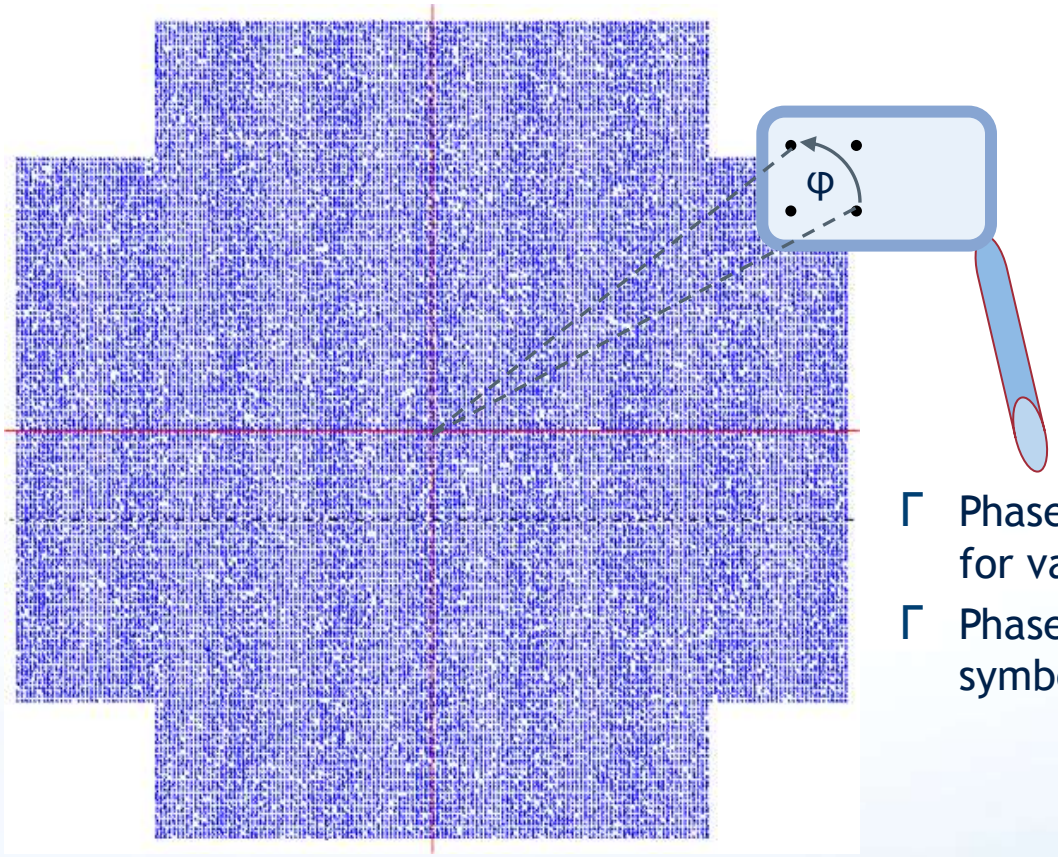
- Cross constellations for
- b=3,5,7,9,11,13,15 bits per symbol

➔8 … 32768 constellation points.

➔Example: b=7, K=128 points

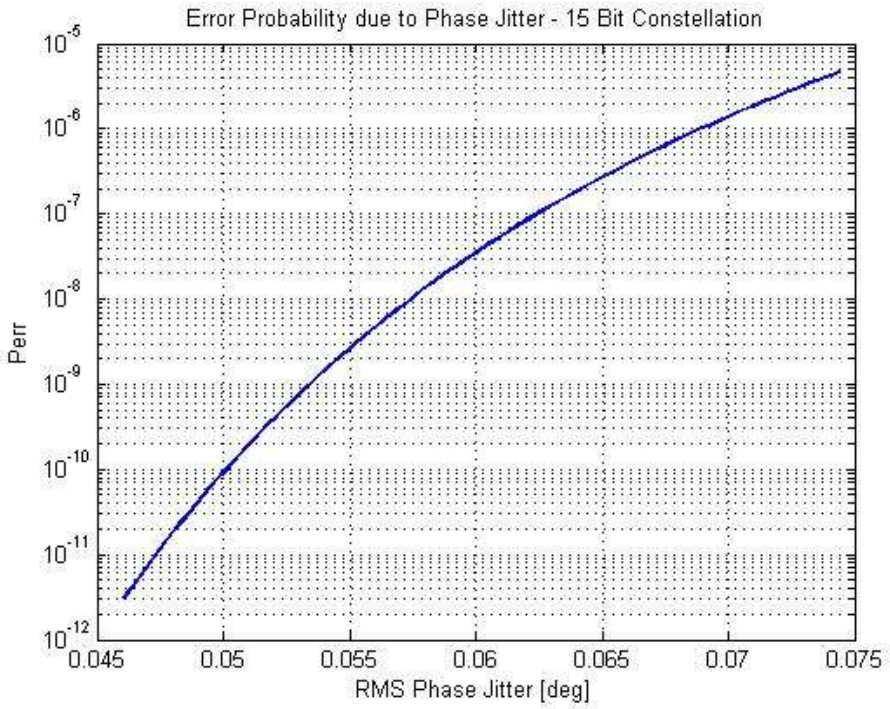
Phase Jitter Impact on dense xDSL Constellation
15 Bit VDSL2 Constellation – 32768 points

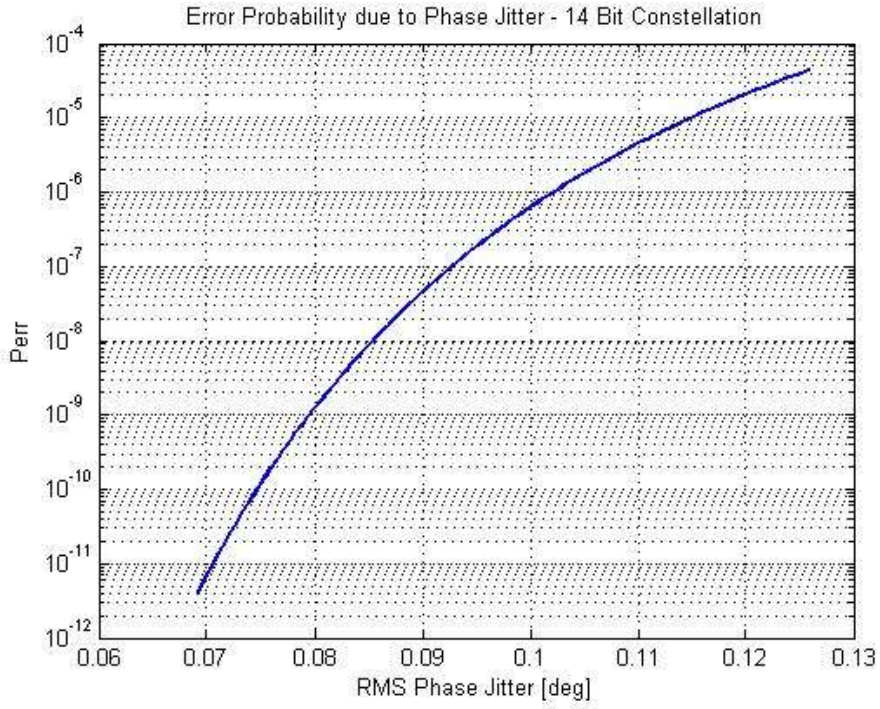
- Measurement of a 15 bit constellation at the VDSL2 receiver



- Phase errors start causing false detections for values as little as $\varphi=0.3^{\circ}$
- Phase errors affect all carriers of a DMT symbol at the same time

Phase Jitter Impact on dense xDSL Constellation
Symbol Error Rate, Error Free Phase Offset Range





- Phase jitter RMS σ_φ for Error Probability $P_{err}=10^{-10}$
  - 14 Bits: $\sigma_\varphi = 1.303*10^{-3}$ rad, i.e., $\sigma_\varphi = 7.463*10^{-2}$ deg
  - 15 Bits: $\sigma_\varphi = 8.541*10^{-4}$ rad, i.e., $\sigma_\varphi = 4.894*10^{-2}$ deg

NTR synchronous to loop timing - Conclusion

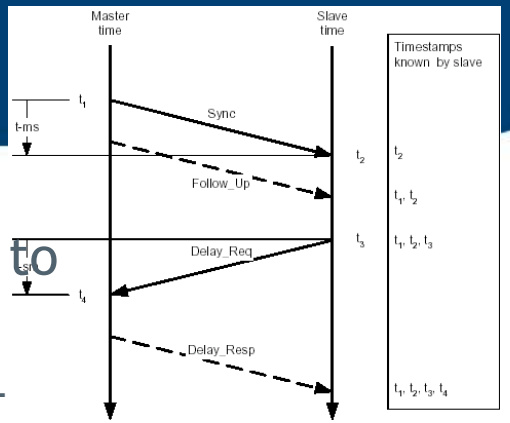
PRO

- Continuous frequency synchronization, free of drift
- Very low phase error due to robustness of DSL loop timing

Challenges

- needs synchronized CO clock-source (35.328MHz, industry standard clock for DSL)
- DSL performance may become dependent on jitter and wander of the network clock
- low-wander CO clocks required, eg. by narrow band PLLs frequency drift (wander) limit of 0.08ppm/s found to be marginal

Why Not Run IEEE1588 across DSL ?
Limitations in QoS



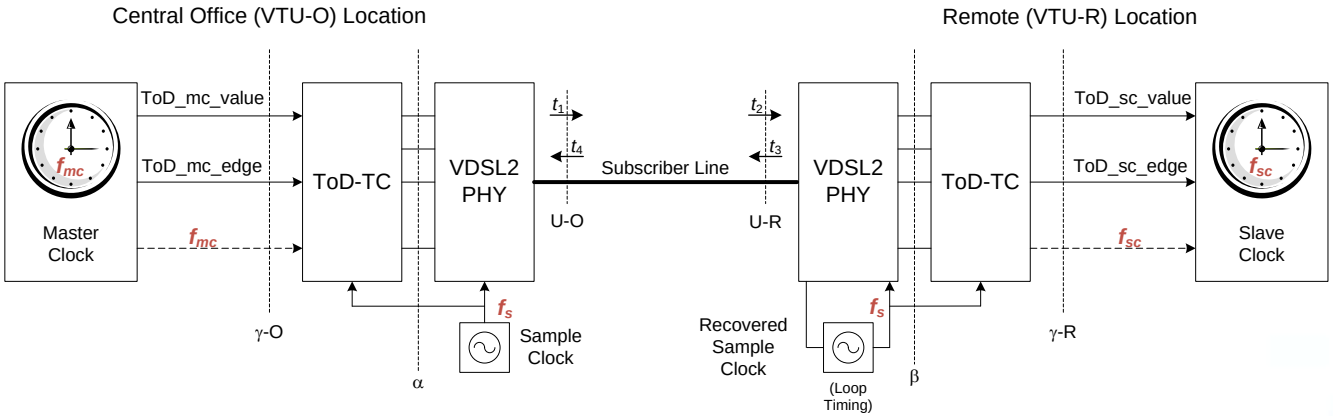
- Applying the IEEE1588 concept of Boundary Clocks to DSL is of limited accuracy:
  - Unlike Ethernet, there is no clearly defined "Start-Of-Packet", "End-Of-Packet" for a PTP protocol frame traversing a DSL link
  - 1588 PTP payload can be treated with priority, but… the DSL PHY is carrying payload in a bursty fashion of unpredictable nature (see box)
- Asymmetrical delays up- and downstream limit the overall PTP accuracy
- Discussion & papers at ITU-T SG15/Q4:
  - no phase sync over DSL using plain 1588 methods possible
  - Started definition of a “xDSL enabled PTP”

Some contributors to DSLs "Burstiness"

- DMT symbol processing (4/8KHz)
- Reed-Solomon Codeword Length (variable)
- Retransmission at Physical Layer (G.998.4)
- Periodic Sync Symbol
- Flow-Control towards Network-Processor
- Online Reconfiguration (Rate Changes)

What is next – IEEE1588 like PTP for VDSL2

ITU-T proposal for IEEE1588 like PTP for VDSL2

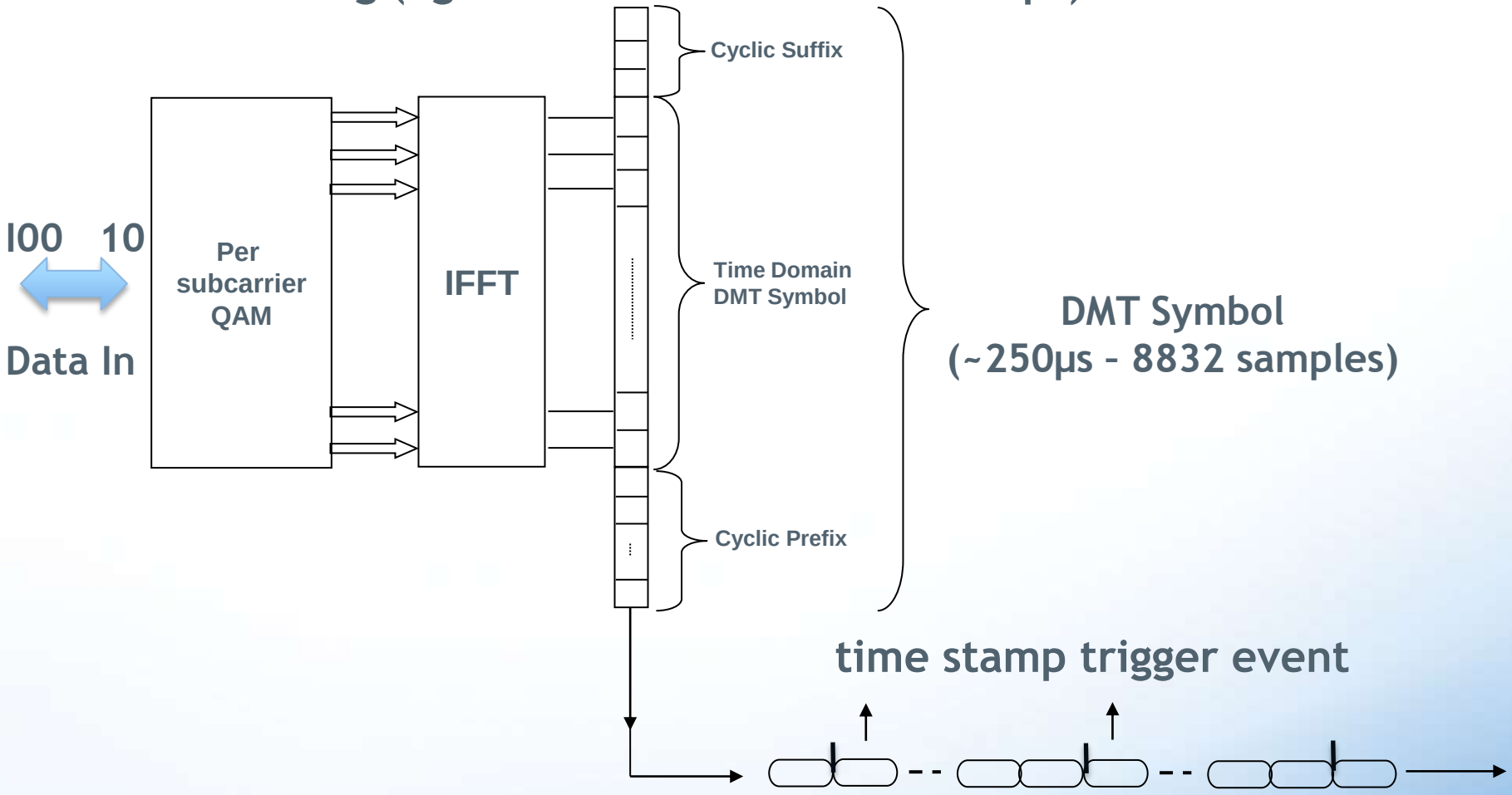


- At VTU-O, time stamps are taken at a dedicated time domain reference sample of particular downstream DMT symbols at the U-O interface
- At VTU-R, time stamps are taken at the reception of the same time domain reference sample of particular DMT symbols at the U-R interface
- Time stamp information is transmitted from VTU-O to VTU-R in the EOC (embedded operation channel) of the VDSL link
- Same mechanisms to be used in upstream direction, i.e. from VTU-R to VTU-O

➔ By linking the time stamp collection to the VDSL2 loop timing, it is possible to achieve almost jitter free time stamp pairs on VTU-O and VTU-R similar to the “start of packet” concept of IEEE1588 for Ethernet systems

Time Stamp Trigger based on xDSL time domain samples

Block Processing (eg. 25000 bit/block @ 100Mbps)



Summary

- ADSL and VDSL support frequency synchronization across the physical layer already since early versions of the standards
- The NTR concept allows to recover clocks at the remote side of DSL links within well known MTIE / TDEV masks as defined in ITU-T G.823
- Synchronous NTR transport may be utilized in ADSL and VDSL2 systems. Since ADSL and VDSL2 use high modulation complexities, the accuracy requirements for the DSL clock generation from of the network clock scheme need careful attention
- At ITU-T – the main standardization body for xDSL transceiver technology– new standards are in definition to allow PTP based ToD transport across xDSL links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