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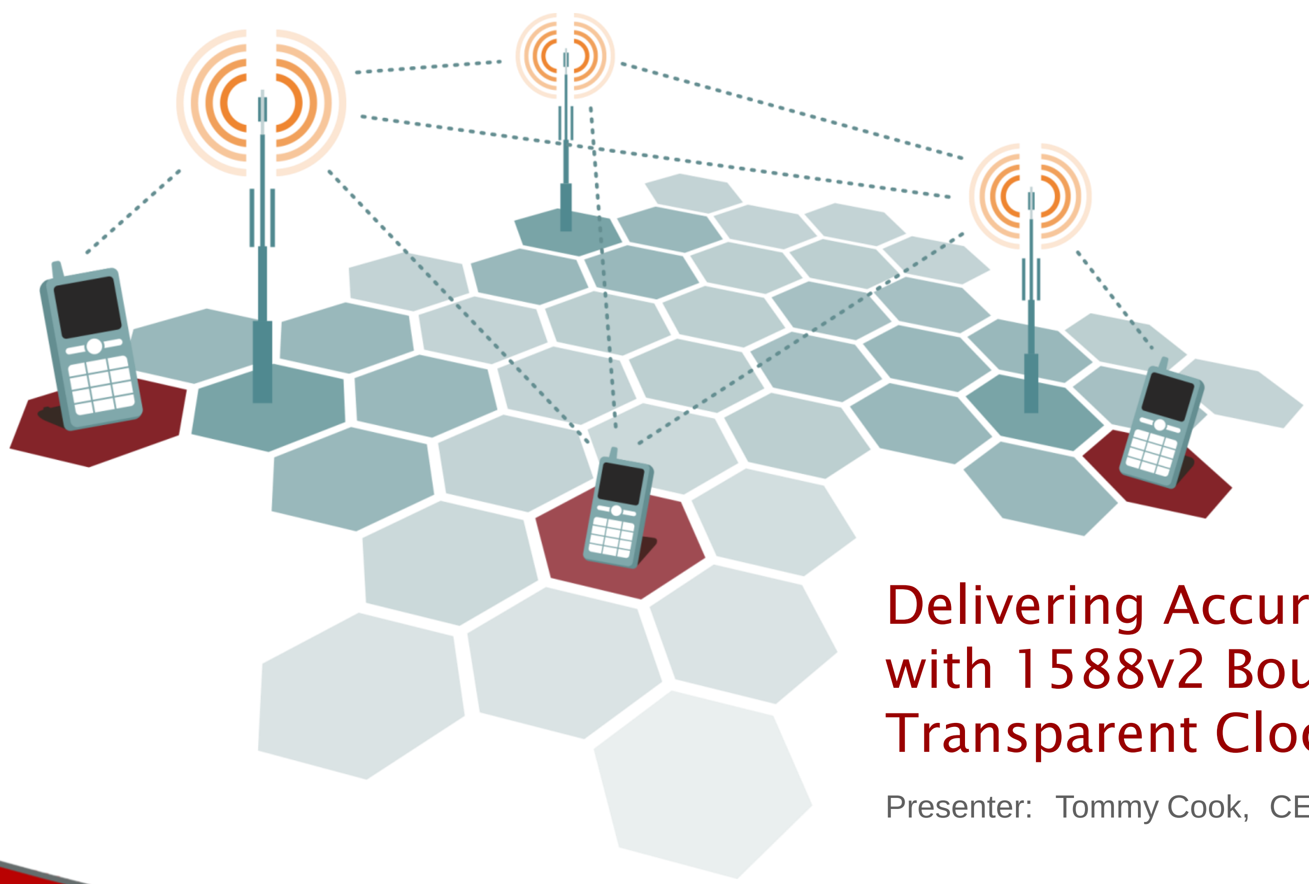


Delivering Accurate Time-of-Day with 1588v2 Boundary Clocks & Transparent Clocks

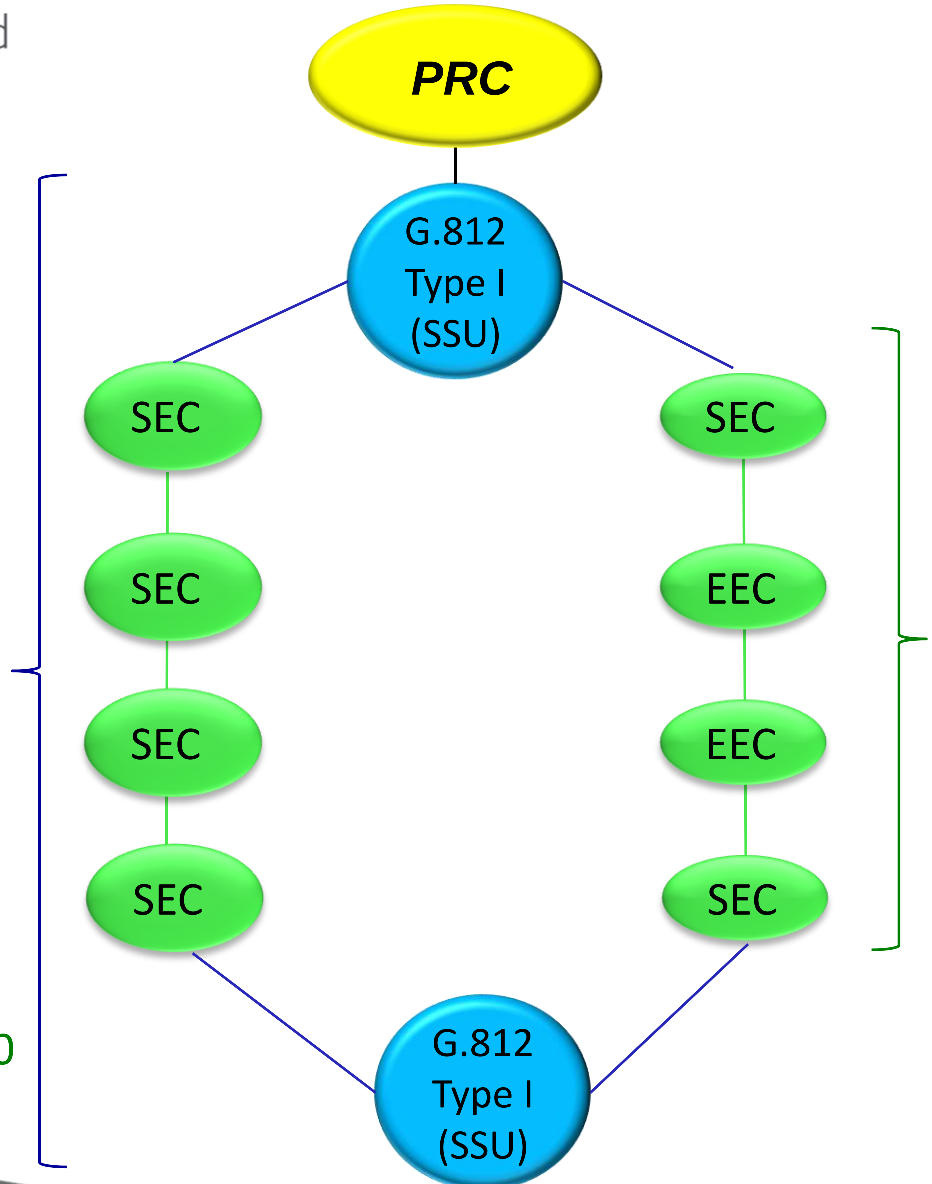
Presenter: Tommy Cook, CEO Calnex Solutions Ltd

Presentation overview

- Traditional approach to building a Timing Network.
- 1588v2 Networks utilising only Ordinary Clocks.
- 1588v2 Networks with On-path Support.
  - Boundary Clocks;
    - Characterising performance of BCs.
    - Building networks of BCs.
  - Transparent Clocks;
    - Characterising performance of TCs.
    - Building networks of TCs.
  - Building your Network with BCs, TCs & Ordinary Clocks.

Building a Timing network

- **ITU-T Standards fully specify the performance requirements for building Networks.**
  - **G.810,** Aug. 1996
    - **Definitions & Terminology for Synchronisation networks**
  - **G.811,** Sept. 1997
    - **Timing Characteristics of Primary Reference Clocks**
  - **G. 812,** June 2004
    - **Timing requirements of slave clocks suitable for use as node clocks in synchronization networks**
  - **G.813,** March 2003
    - **Timing characteristics of SDH equipment slave clocks (SEC)**
  - **G.8262,** July 2010
    - **Timing characteristics of a synchronous Ethernet equipment slave clock**



Number of G.812 type I clocks ≤ 10

Number of G.813 option 1 clocks ≤ 20

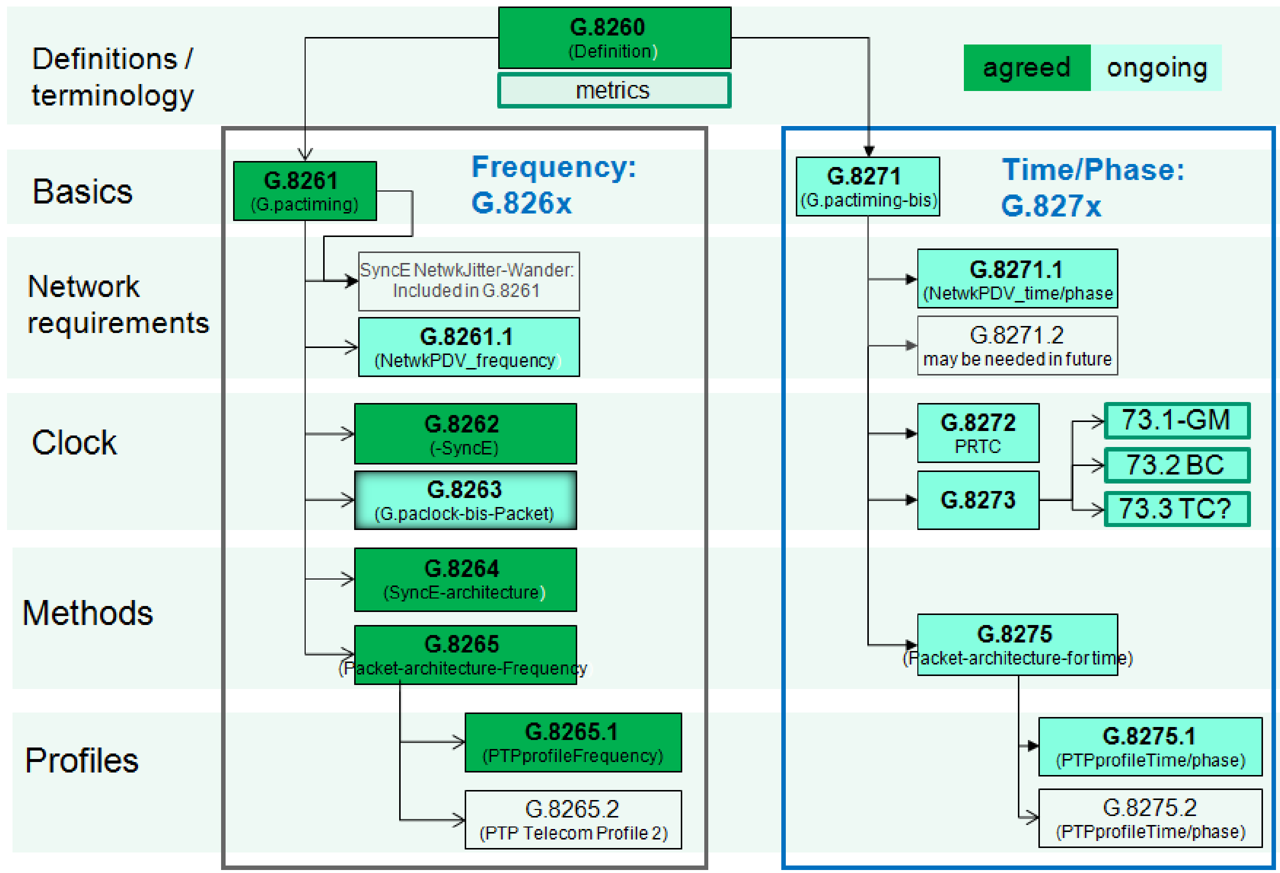
Total number of G.813 clocks in a sychronisation trail should not exceed 60

G.8262 is Compatible with G.813

EEC – Ethernet Equipment Clock

Building a Network with 1588v2

- IEEE 1588-2008 version 2.
  - **IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems**
  - Provides a **functional** description of devices that can use 1588v2 to transfer time and frequency using timestamps.
  - This document is not application specific.
- ITU-T Standards specify the use of 1588v2 in the Telecoms applications.



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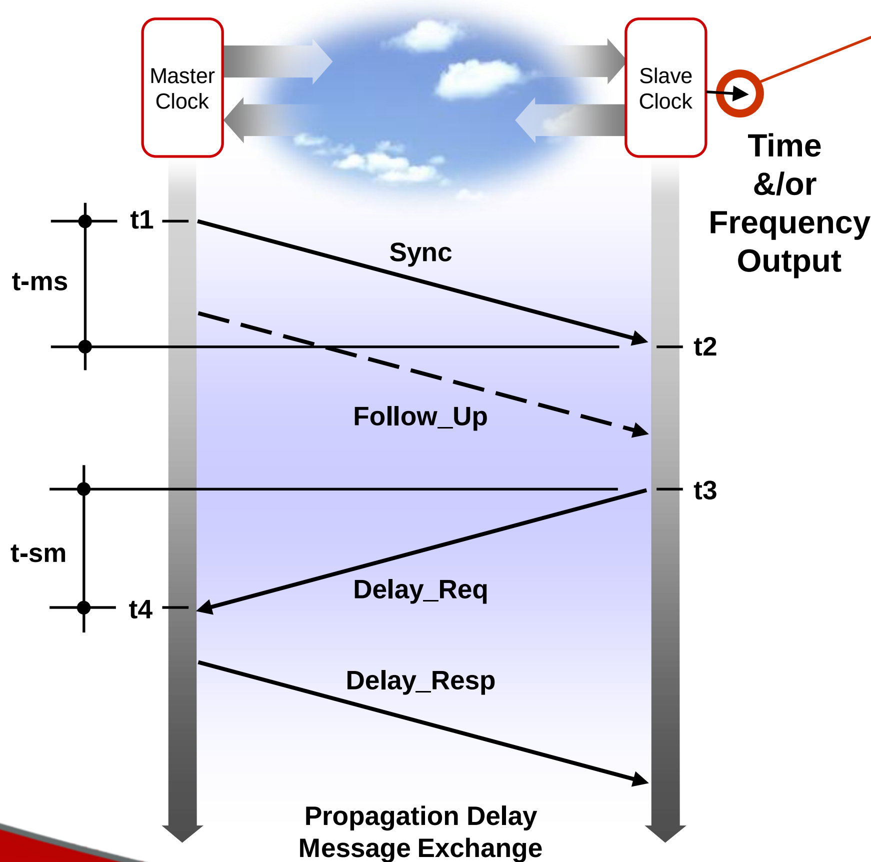
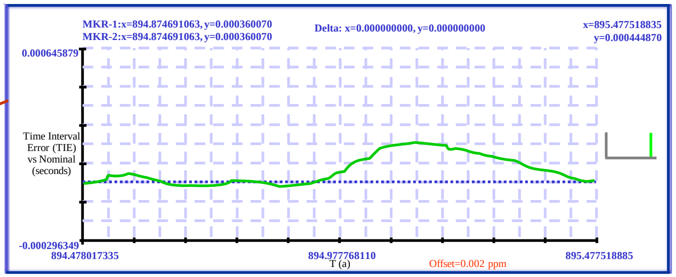
Performance objectives of 1588v2 network





- **Performance is specified on the Time &/or Frequency output from the Slave clock.**
- **Frequency Output must comply with the relavent ITU-T interface specification, (MTIE & TDEV specification);**
  - **G.823/4 Traffic Interface Masks.**
  - **G.823/4 Sync Interface Masks.**
- **Time output must comply with end application requirements.**
  - **1pps output**
  - **Time error in µsec**

Setting Expectations …

What Does 1588 Aim To Achieve?

Version 1

- 1 microsecond time-of-day precision over Industrial Ethernet (±0.5 µS)

1588v2

- less than 100 nanosecond (target 50nS) time-of-day precision over Ethernet LAN.
- Less than 1µs time-of-day precision over switched Ethernet WAN.
- stable frequency ($1.6x10^{-8}$ or 16ppb) recovery (from time-of-day reference).

What Do Mobile Networks Need?

Application	Frequency	Time
CDMA2000	±50 ppb	Goal: <3µs Must Meet: <10µs
GSM	50 ppb	N/A
WCDMA	50 ppb	N/A
TD-SCDMA	50 ppb	3µs inter-cell phase difference
LTE (FDD)	50 ppb	N/A
LTE (TDD)	50 ppb	**3µs inter-cell phase difference
LTE MBMS	50 ppb	**5µs inter-cell phase difference
FemtoCell	250 ppb	N/A
WiMAX (TDD)	2 ppm absolute, ~50 ppb between base stations	Typically 1 – 1.5 µs
Backhaul N/W	16 ppb	N/A

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1588v2 Networks utilising only Ordinary Clocks

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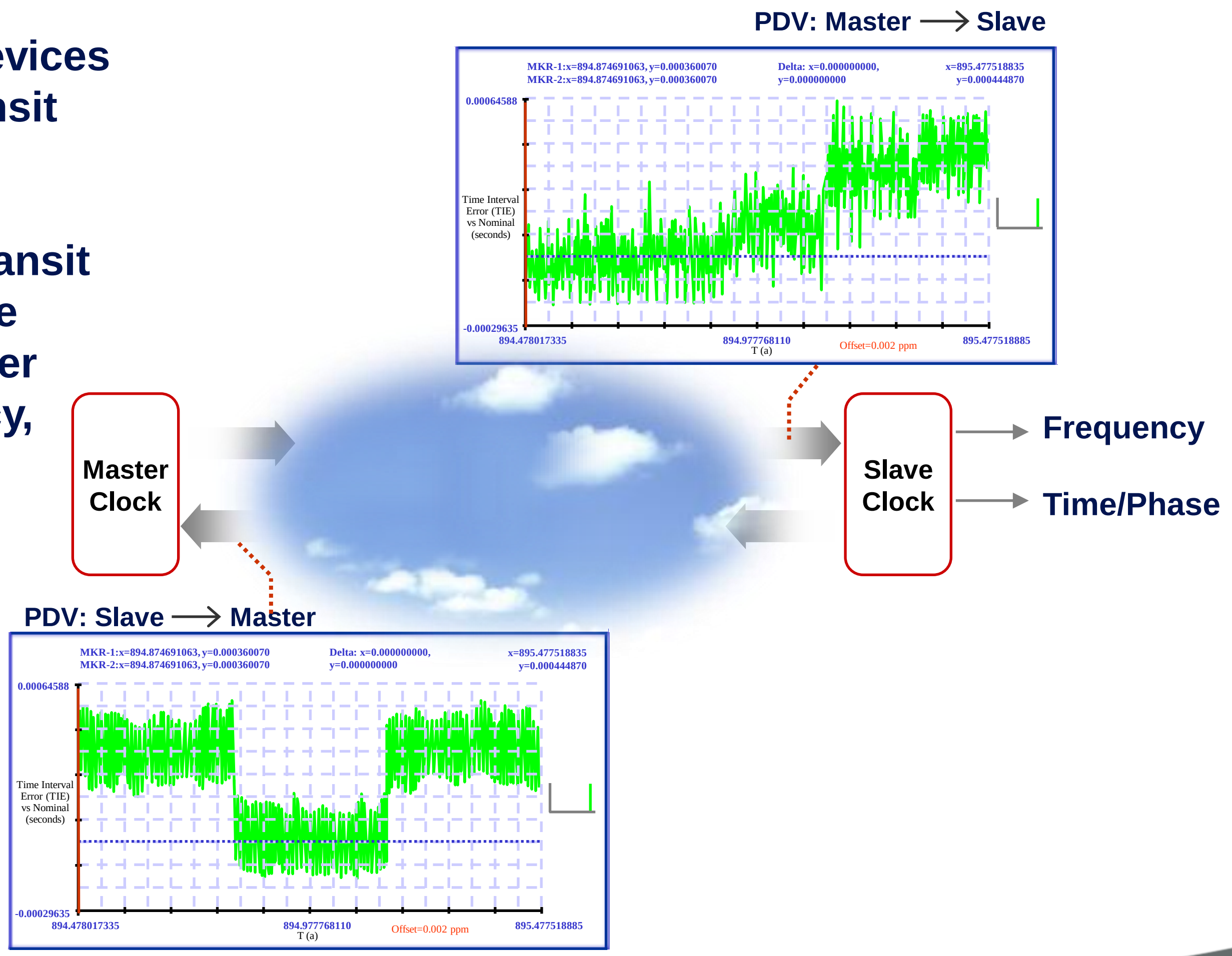
The role of 1588v2 Ordinary Clocks

- **Master;**
  - **Source of 1588v2 Message flow which contains the timestamp information on Master's reference clock.**

- **Slave;**
  - **Destination of a 1588v2 message flow where the timestamps are used to recover the time, phase &/or frequency of Master's reference clock.**

The impact of the Network on 1588v2

- **Congestion in network devices results in variation of transit time for each packet.**
- **The more disruption to transit time, the more difficult the task of the Slave to recover and align to the Frequency, Time &/or Phase of the Master Clock.**



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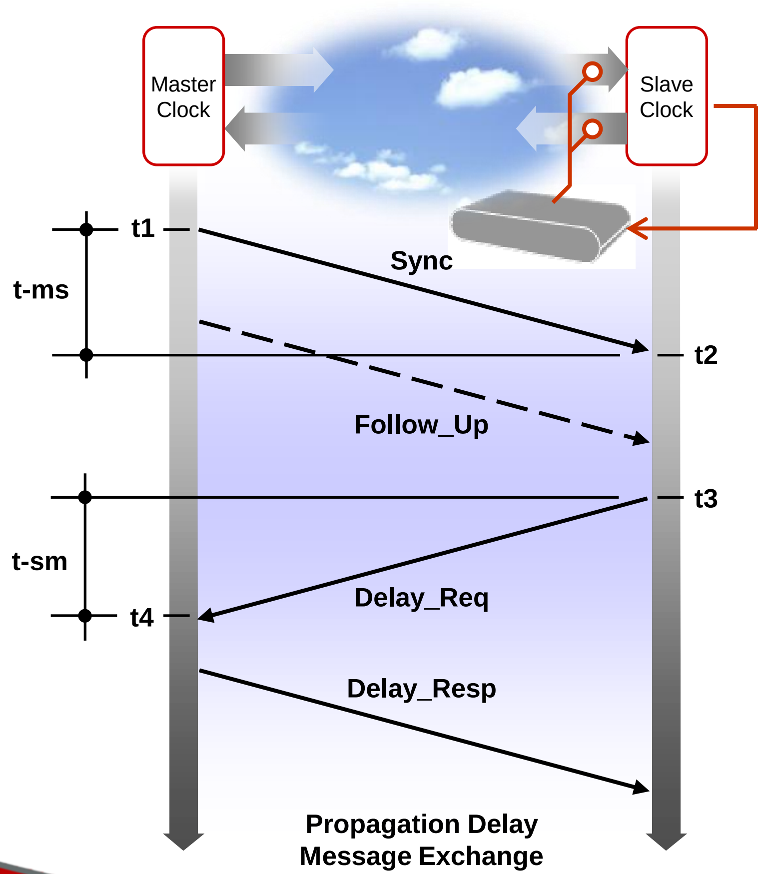
What impacts 1588v2 Slave timing accuracy?



Monitor Slave performance
- **1pps: Time**
- **T1/E1: Frequency**

There are many characteristics of the 1588v2 message flows that can impact the quality of the recovered Time &/or Frequency:

- **Key characteristics that affect timing recovery:**
  - **Sync PDV**
    - with Follow-up
    - with Correction Factor
  - **Delay_Req PDV**
- **Secondary characteristics that may affect timing recovery:**
  - Round Trip Delay (Sync + Delay_Req)
  - Path Asymmetry
  - Delay_Req Response Time
  - Sync IPG
  - Follow-up PDV

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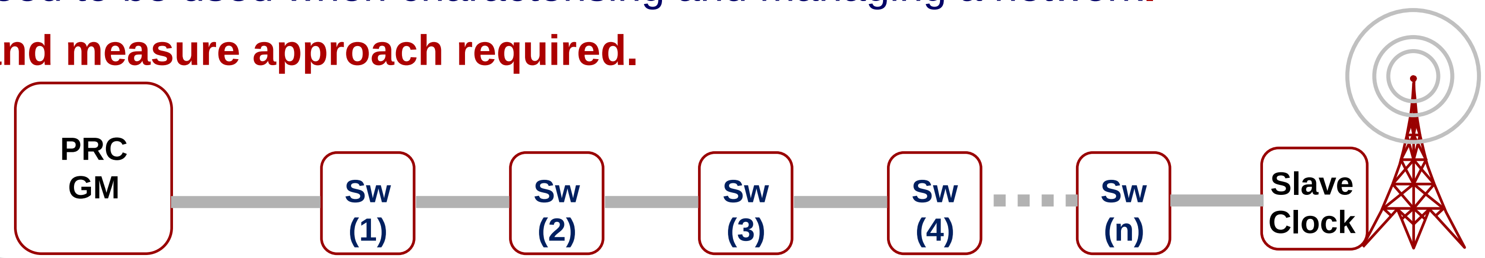
Networks with non-‘1588v2 aware’ switches

- **The ‘G.81x approach’ offers a Standards-based structured, bottom-up approach.**
  - The performance of each device in the path is know and has been proven.
  - Adhere to topology guidelines and the resulting network performance **will be within defined performance limits.**
- **With non-1588v2 aware switches, this is not possible today.**
  - While work is on-going in ITU-T SG15, Q.13, today there is no agreed method to measure and quantify a Ethernet Switches PDV performance.
- **Today’s approach is for the Slave vendor to specify the approach to be employed.**
  - Build, test and potentially monitor networks to measure the total PDV produced.
  - Slave vendors provide Network Operators guidance on which metrics/measures and limits need to be used when characterising and managing a network.
  - **Build and measure approach required.**



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Networks with on-path support

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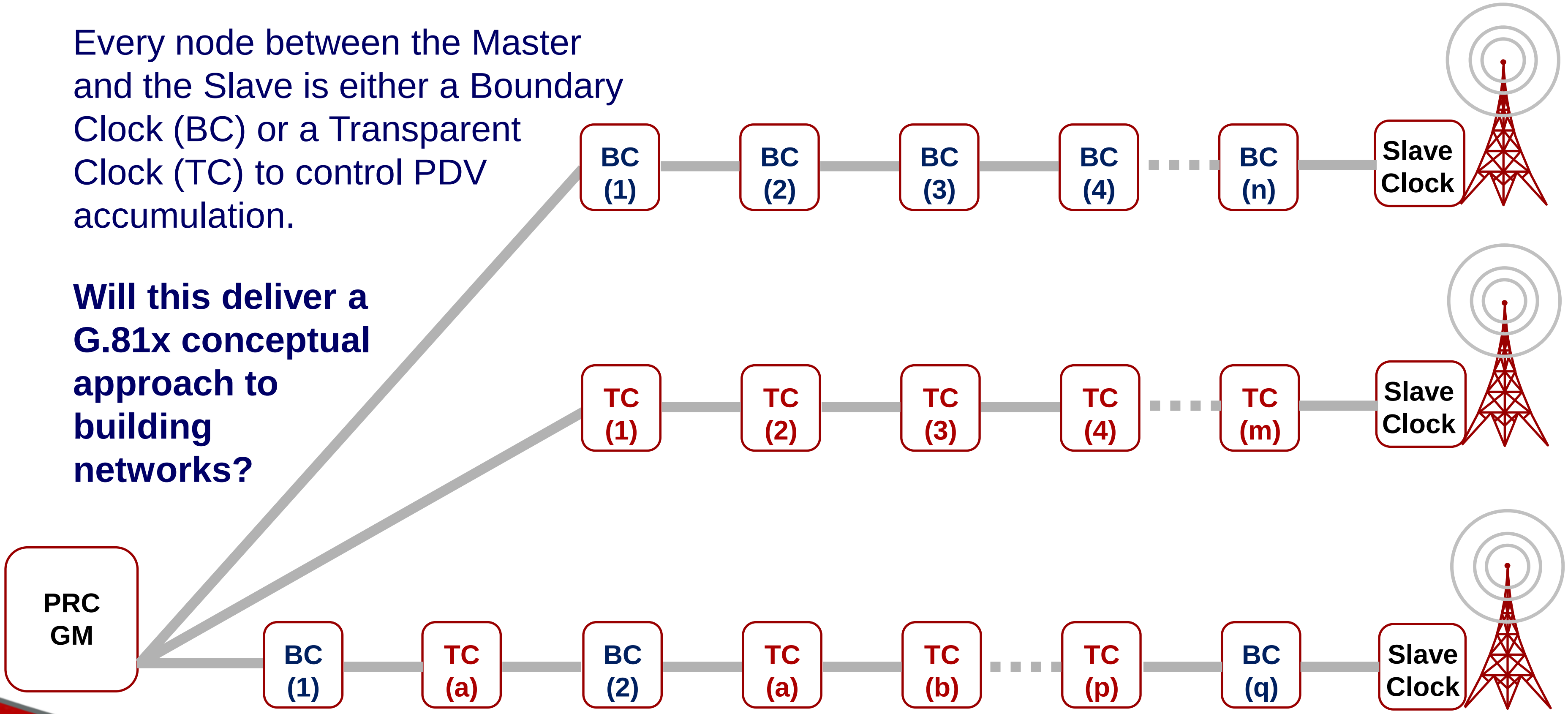
Design your network with Full On-path Support

Every node between the Master and the Slave is either a Boundary Clock (BC) or a Transparent Clock (TC) to control PDV accumulation.

Will this deliver a G.81x conceptual approach to building networks?



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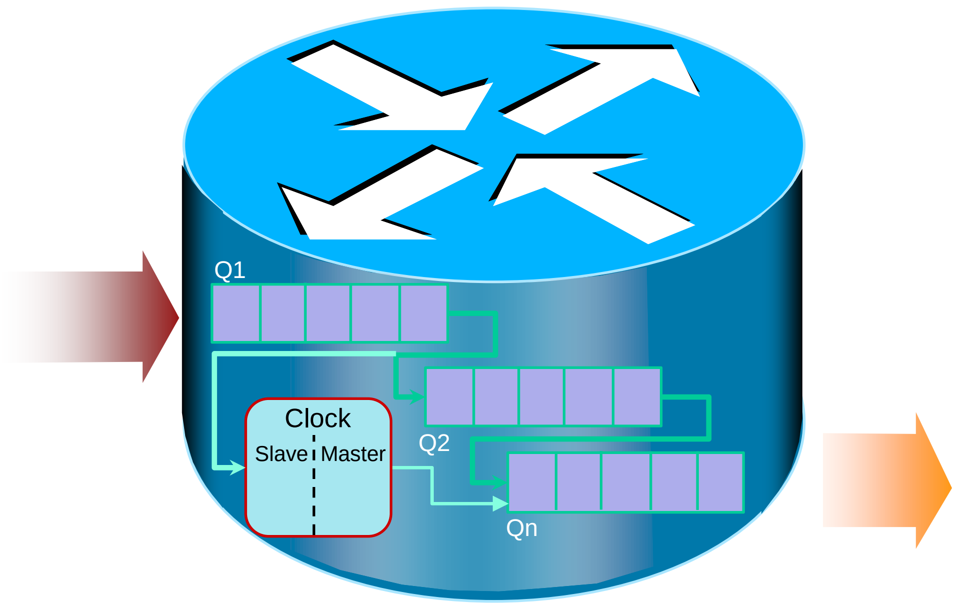
Boundary Clocks

Boundary Clock

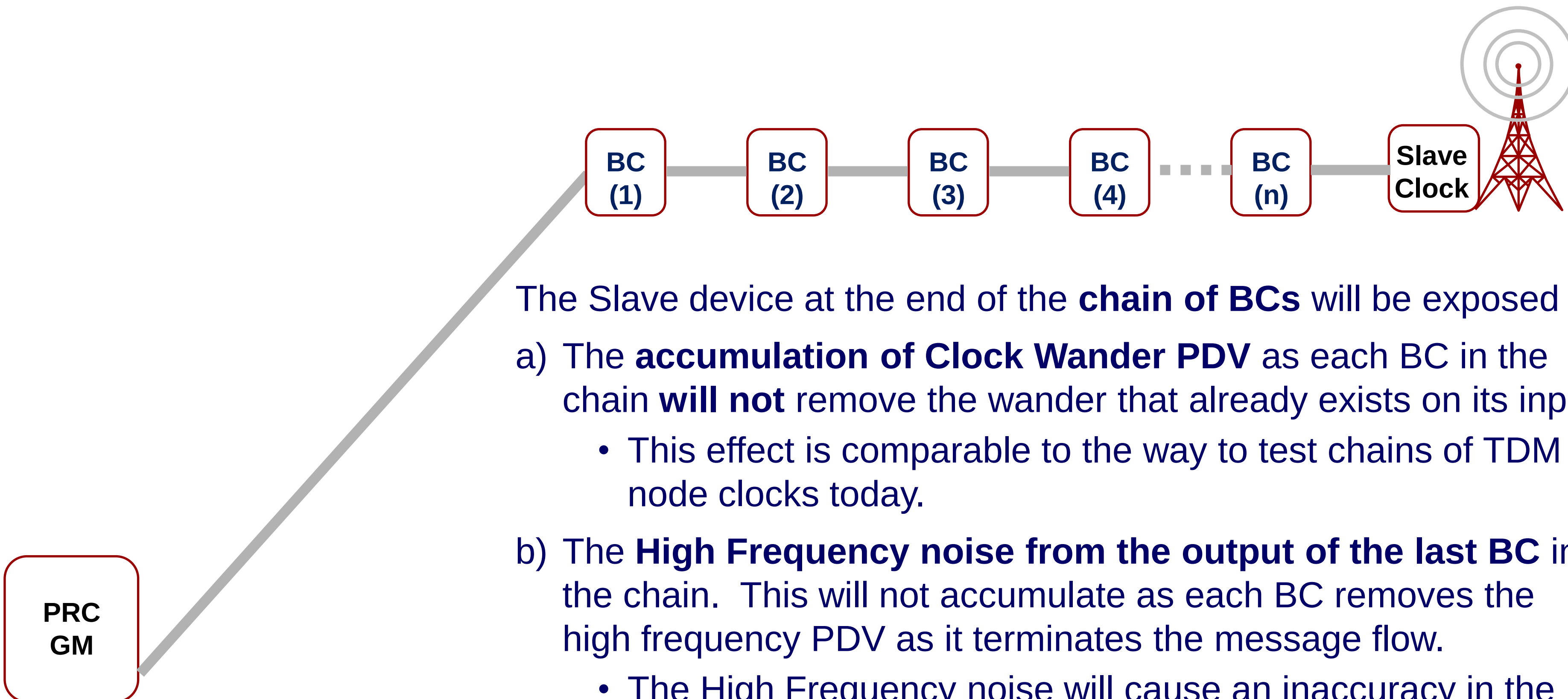


Boundary Clocks reduce PDV accumulation by;

- Terminates the PTP flow and recovers the reference timing.
- Generate a new PTP flow using the local time reference, (which is locked to the recovered time).
- No direct transfer of PDV from input to output.

Boundary Clock is in effect a back-to-back Slave+Master.

Design your network with Full On-path Support



The Slave device at the end of the **chain of BCs** will be exposed to;

a) The **accumulation of Clock Wander PDV** as each BC in the chain **will not** remove the wander that already exists on its input.
   - This effect is comparable to the way to test chains of TDM node clocks today.

b) The **High Frequency noise from the output of the last BC** in the chain. This will not accumulate as each BC removes the high frequency PDV as it terminates the message flow.
   - The High Frequency noise will cause an inaccuracy in the recovery of time in each BC. This is for further study

c) The combination of a) & b) together.

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Transparent Clocks

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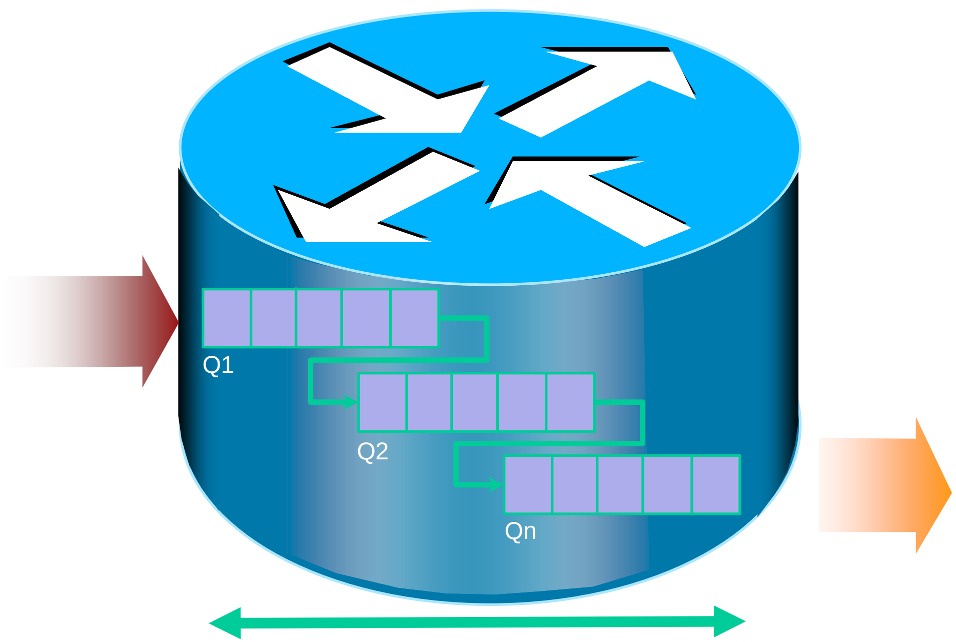
Transparent Clock

Transparent Clocks reduce PDV by;

- Calculating the time a PTP packet resides in the TC device (in nsec) and insert the value into the correctionField.
- By using the correctionField, the Slave or terminating BC can effectively remove the PDV introduced by the TC.



Packet Delay in TC Device
inserted into correctionField
at output of Transparent Clock device

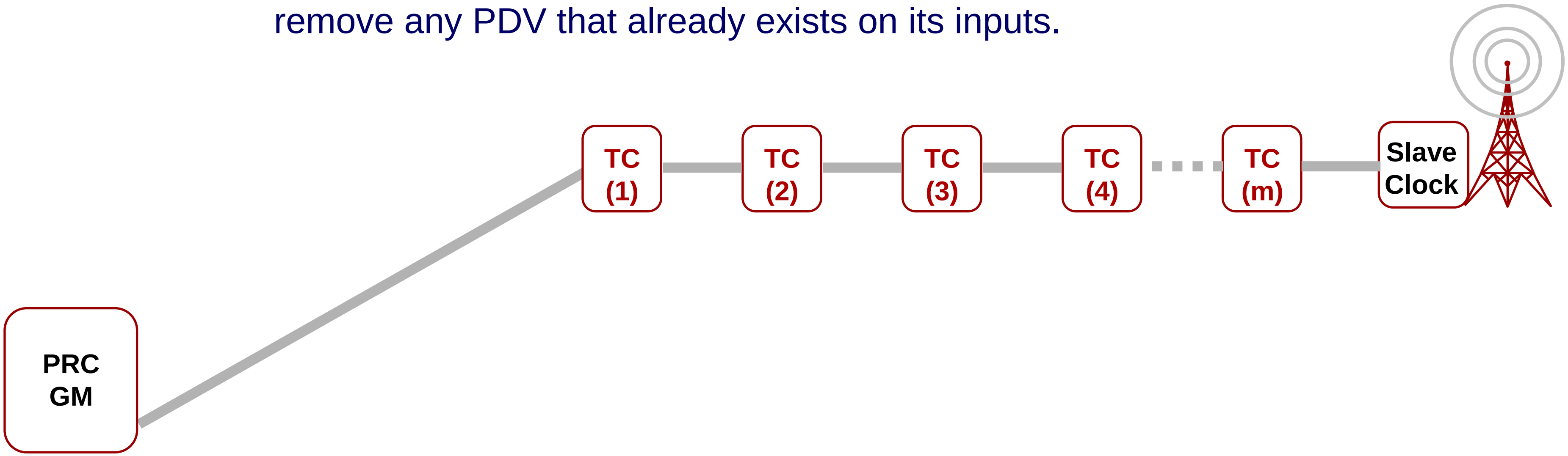
PTP Message Header Format

Bits							
7	6	5	4	3	2	1	0
transportSpecific				messageType			
Reserved				versionPTP			
messageLength							
domainNumber							
Reserved							
Flags							
correctionField							
Reserved							

Design your network with Full On-path Support

The Slave device at the end of the **chain of TCs** will be exposed to;

- The **accumulation of PDV produced by each TC's inaccuracy** as each TC only corrects for the PDV noise it produces, it can not remove any PDV that already exists on its inputs.

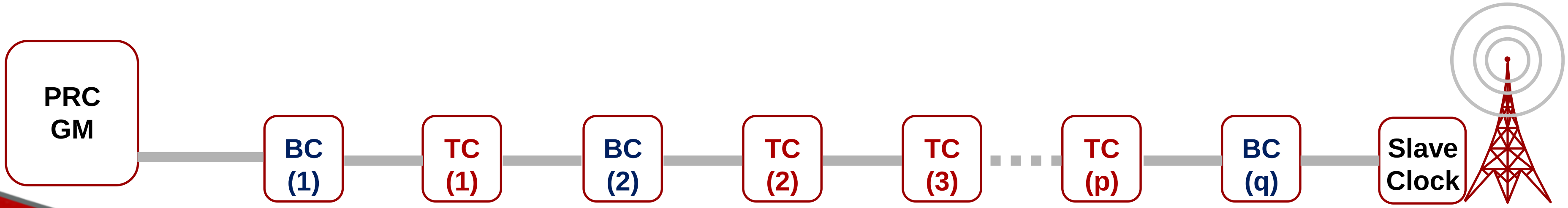


Design your network with Full On-path Support

The Slave device at the end of the **chain of a mix of BCs & TCs** will be exposed to;

- The combined effects of BCs and TCs as described previous. The actual behaviour will depend on the specific combination and ordering of the BCs and TCs in the chain.

The testing of BC and TC when transferring time is currently the subject of discussion in ITU-T SG15, Q13.



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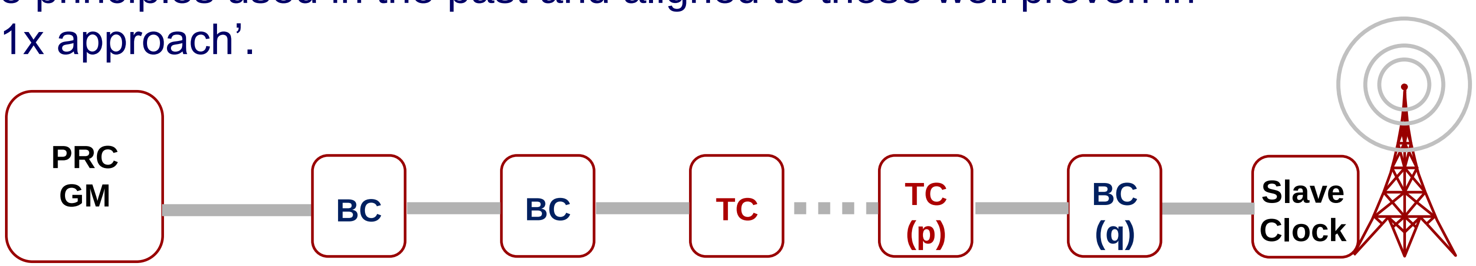
Networks with '1588v2 aware' switches

- **The 'G.81x approach' offers a Standards-based structured, bottom-up approach.**
  - The performance of each device in the path is know and has been proven.
  - Adhere to topology guidelines and the resulting network performance **will be within defined performance limits.**
- **With full On-path support of 1588v2 aware switches, it should be possible to deliver packet networks using a 'G.81x approach'.**
  - Work on-going in ITU-T SG15, Q.13 to simulate networks of BCs with the objective of specific performance requirements of individual and chains of BCs.
  - Once in place, then BCs can be qualify and provided the guidelines to building networks is adhered to, it should be possible to build timing networks using the principles used in the past and aligned to those well proven in the 'G.81x approach'.



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Calnex Paragon Sync

- IEEE 1588v2
- CES
- Sync-E
- OAM