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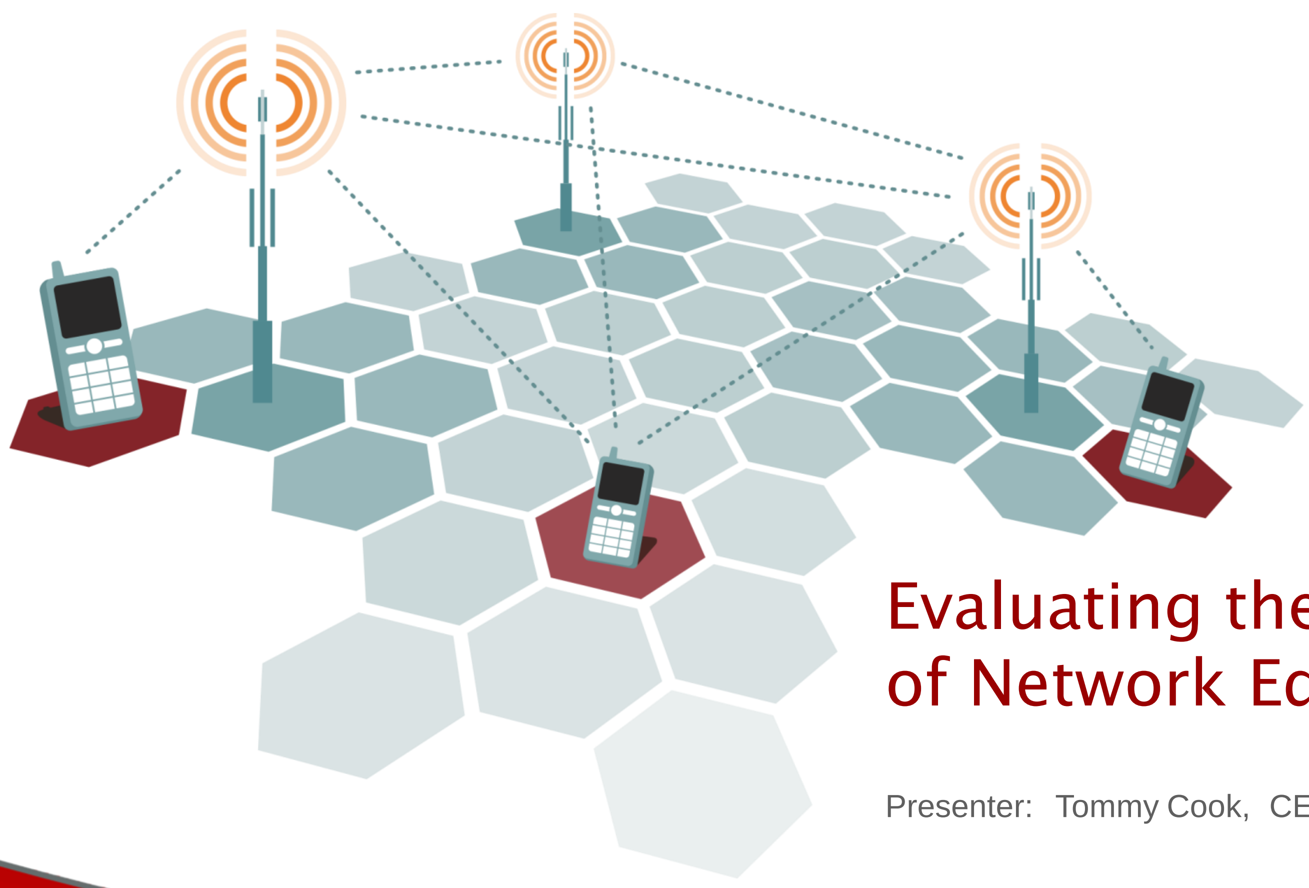

Evaluating the performance of Network Equipment

Presenter: Tommy Cook, CEO Calnex Solutions Ltd

Presentation overview

- **Proving performance of;**
  - **EEC – Synchronous Ethernet Devices.**
  - **1588v2 Boundary Clocks.**
  - **1588v2 Transparent Clocks.**
  - **1588v2 Ordinary Clocks.**
  - **Networks carrying 1588v2.**

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EEC – Synchronous Ethernet devices

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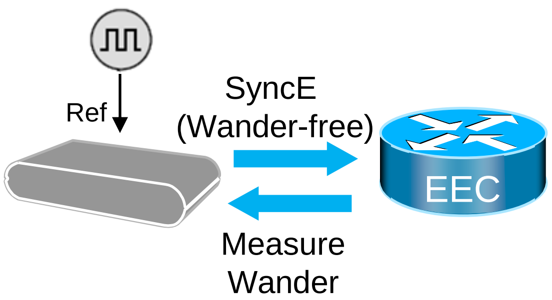
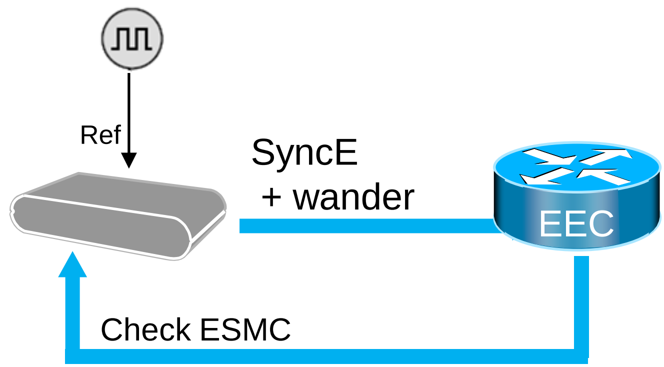
Sync-E Wander to ITU-T G.8262

1) Wander generation

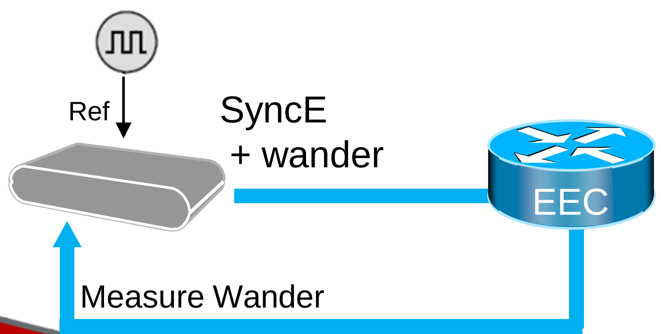


2) Wander tolerance

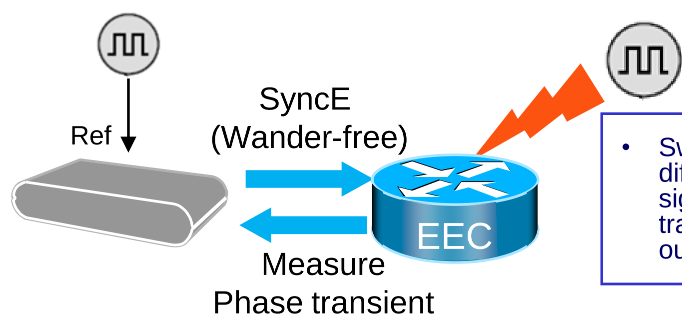


- Maintain clock within performance limits.
- Not causing any alarms.
- Not causing the clock to switch reference.
- Not causing the clock to go into holdover.

3) Wander transfer



4) Phase transient response



- Switching between different synchronization signals results in phase transients at the EEC output

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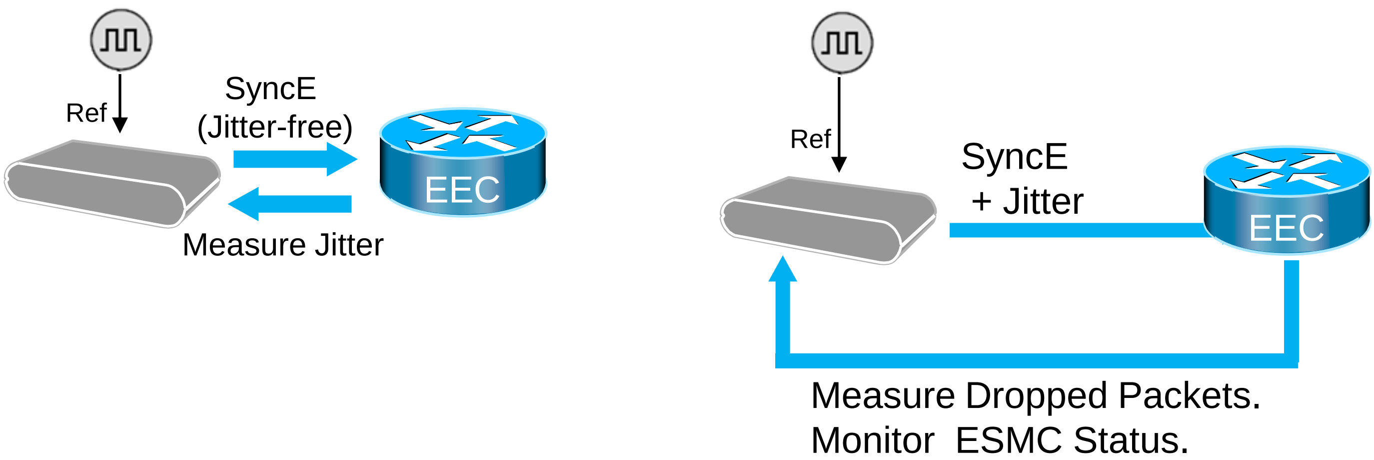
Sync-E Jitter to ITU-T G.8262

1) Jitter generation

2) Jitter tolerance



- No dropped packets indicating bit errors being introduced.
- Not causing any alarms.
- Not causing the clock to switch reference.

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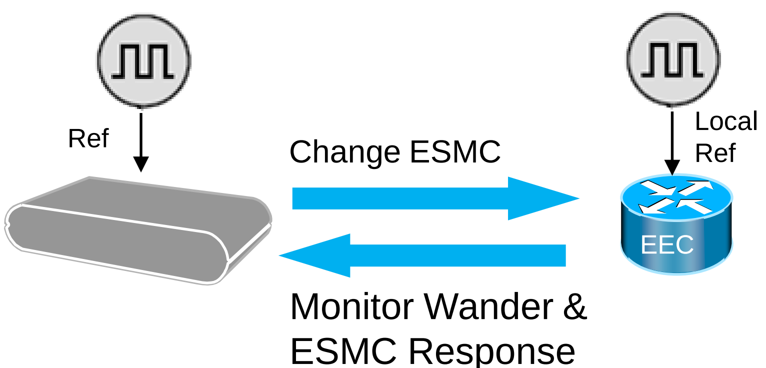
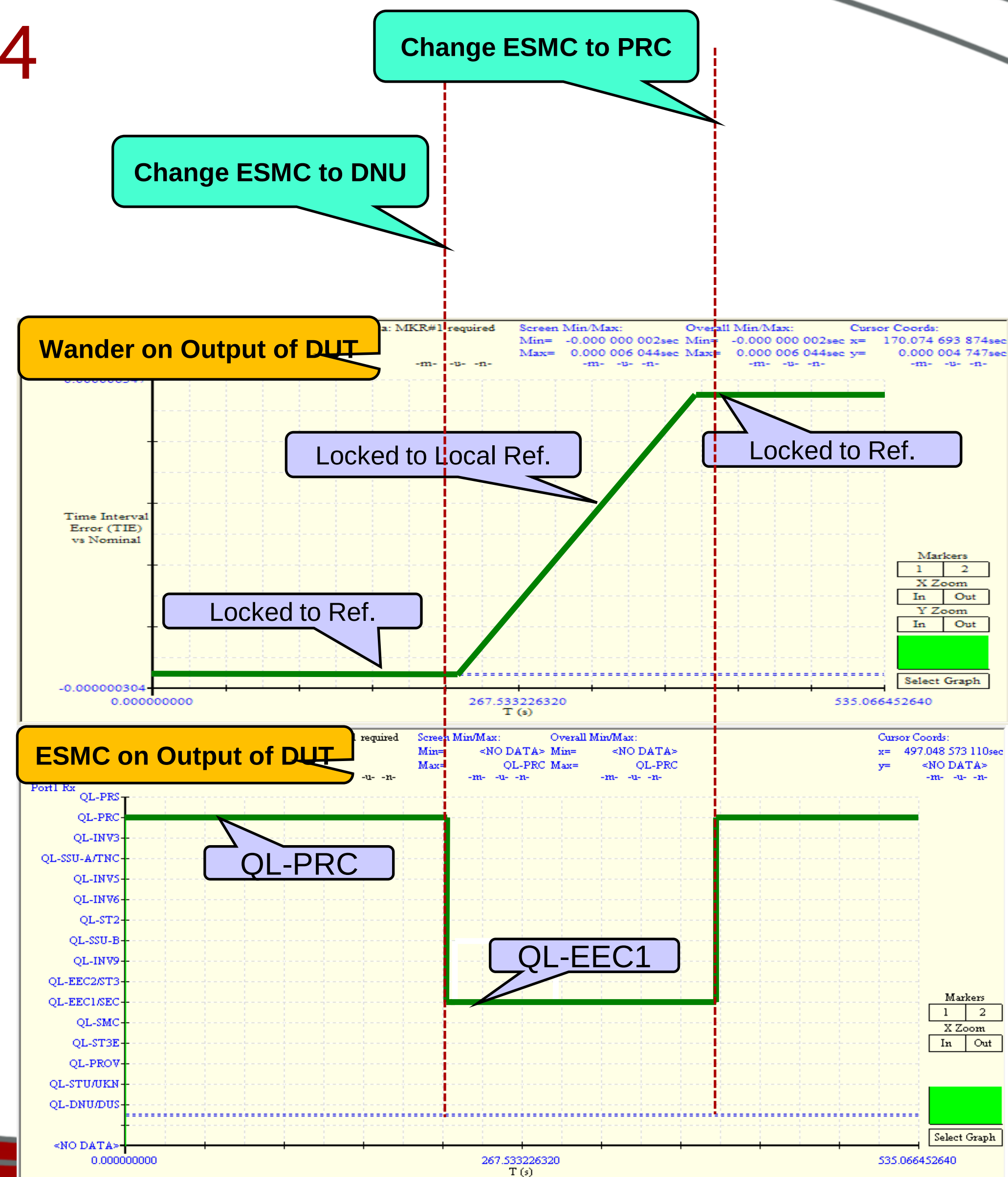
ESMC to ITU-T G.8264

1. **Change the ESMC status being received by EEC.**
2. **Verify ESMC response, and prove EEC also switches clock source by monitoring Wander.**





1588v2 Devices

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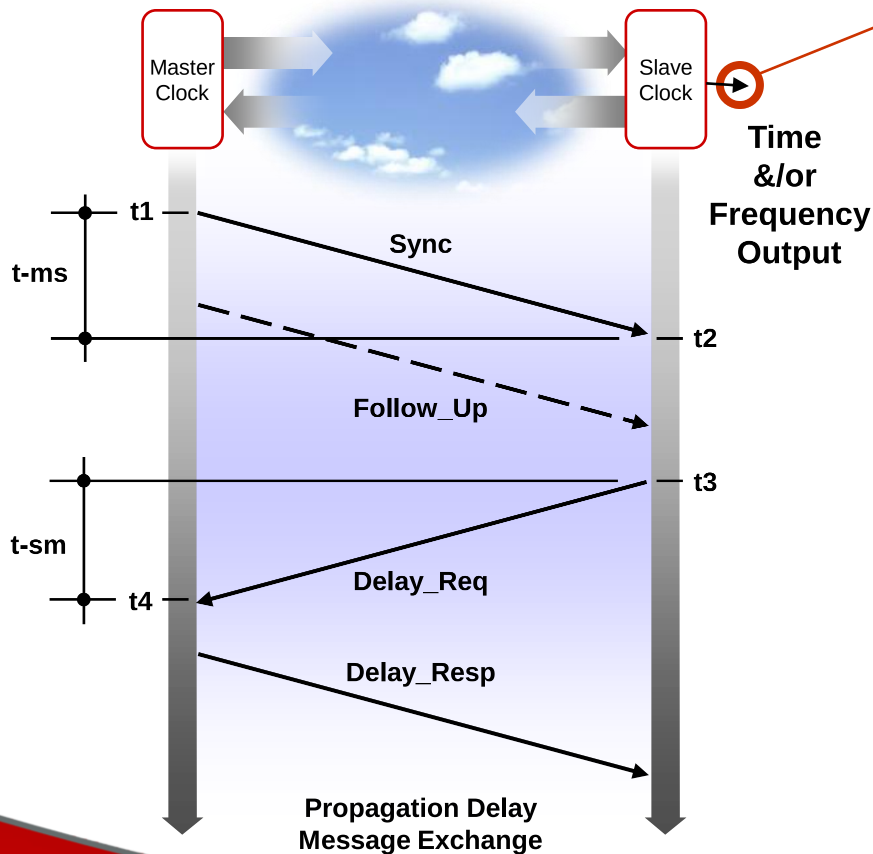
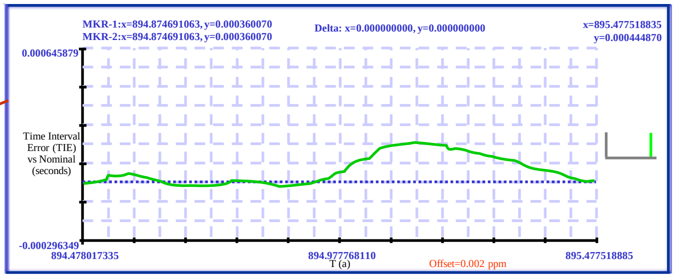
Performance objectives of 1588v2 network

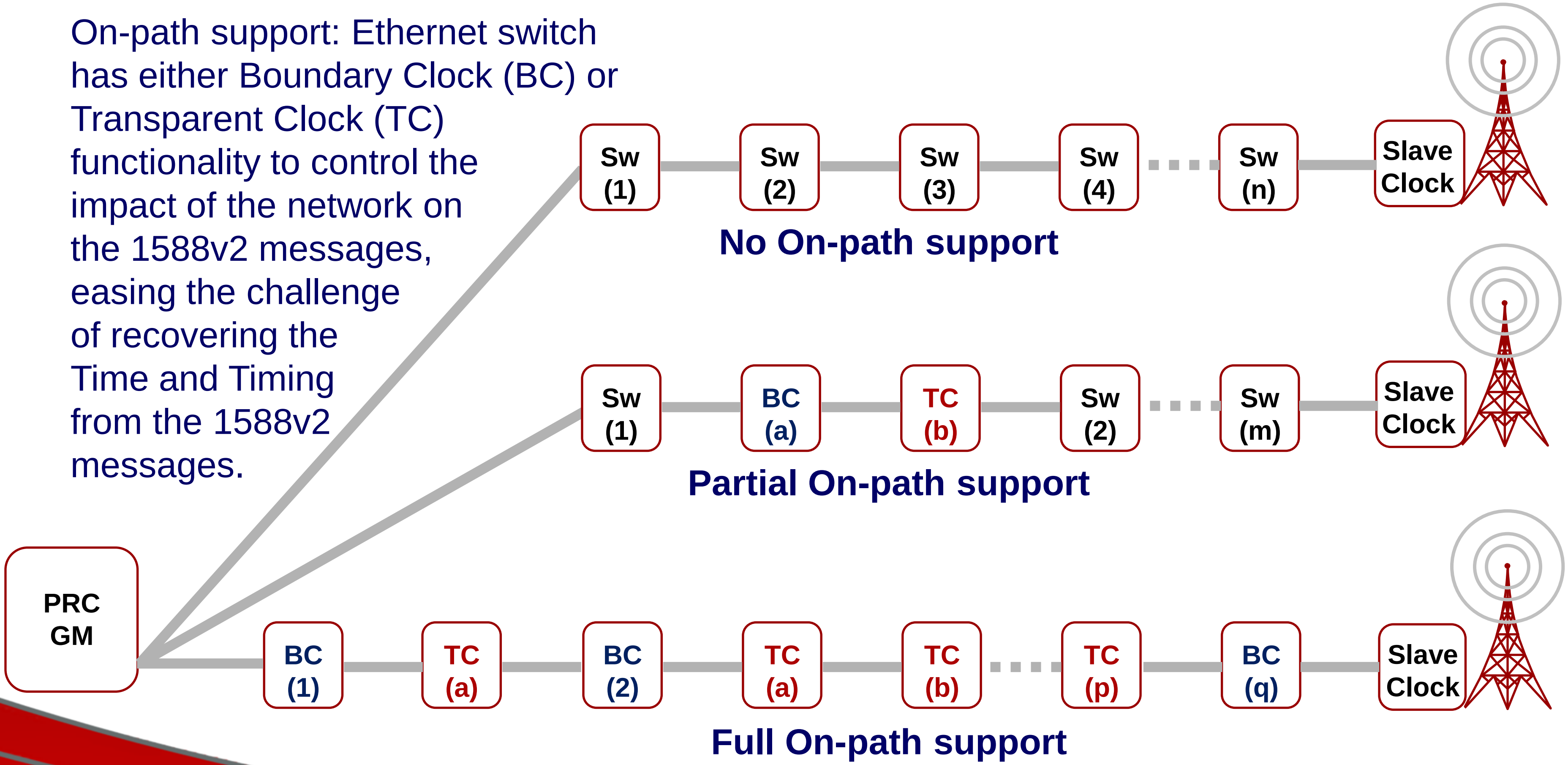




- **Performance is specified on the Time &/or Frequency output from the Slave clock.**
- **Frequency Output must comply with the relavent ITU-T interface specification, (MTIE & TDEV specification);**
  - **G.823/4 Traffic Interface Masks.**
  - **G.823/4 Sync Interface Masks.**
- **Time output must comply with end application requirements.**
  - **1pps output**
  - **Time error in μsec**

Designing your network

On-path support: Ethernet switch has either Boundary Clock (BC) or Transparent Clock (TC) functionality to control the impact of the network on the 1588v2 messages, easing the challenge of recovering the Time and Timing from the 1588v2 messages.



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Boundary Clocks

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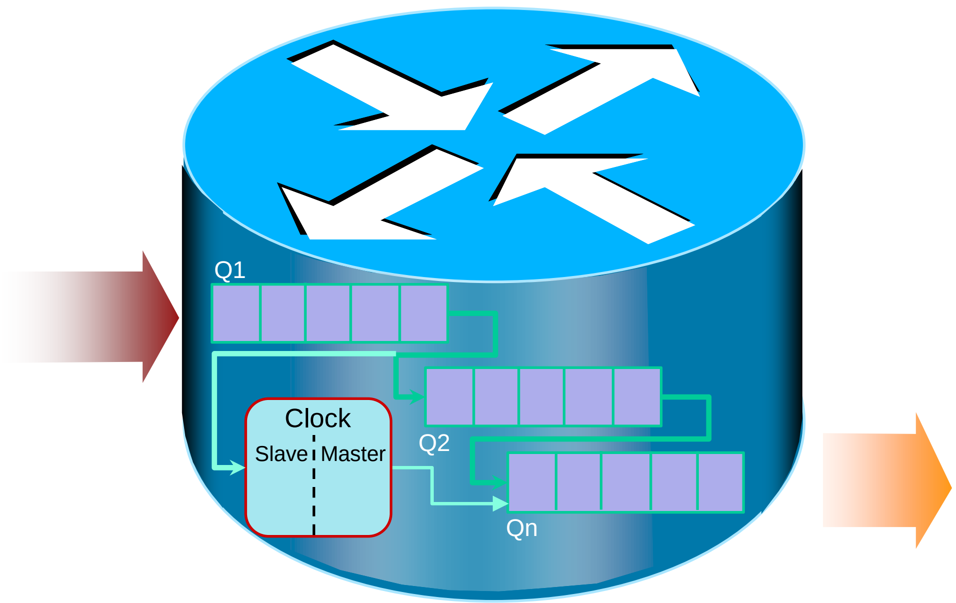
Boundary Clock



Boundary Clocks reduce PDV accumulation by;

- Terminates the PTP flow and recovers the reference timing.
- Generate a new PTP flow using the local time reference, (which is locked to the recovered time).
- No direct transfer of PDV from input to output.

Boundary Clock is in effect a back-to-back Slave+Master.

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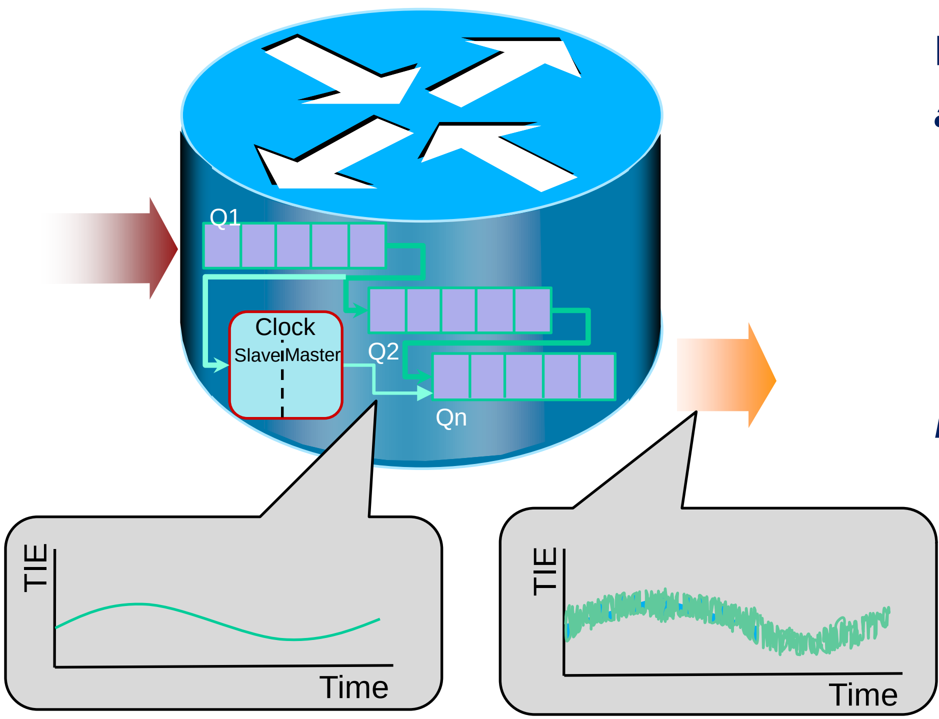
Sources of PDV from Boundary Clock



Regenerated Clock vs. GrandMaster Clock

Output PDV

Potential Sources of PDV;

a) Clock Wander;

- Each BC recovers the clock and re-generates a new timing signal. This can lead to the introduction of low frequency clock wander,
- Chains of BCs can lead to the accumulation of low-frequency clock wander.

b) High-freq. PDV from internal BC packet management;

- PDV from **Output Buffer Queue** of BC;
  - 12 µsec for 1514 Byte packet, (G.8261).
  - 525 µsec for 64K Jumbo Byte packet
- PDV from other internal queues.
- Affected by other High Priority Traffic?

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Performance specification of a BC

Draft ITU-T **G.8273.2** will specify the performance of a BC. Four sections have been proposed;

6. Noise Generation

7. Noise Tolerance

8. Noise Transfer

9. Phase Transient and Holdover Response

The approach being taken in G.8273.2 is following the well established methods of specifying the performance of node clocks (e.g. in G.8262 for SyncE, etc.)

The impact of congestion traffic on the output PDV may require an additional test;

X. Impact of congestion traffic

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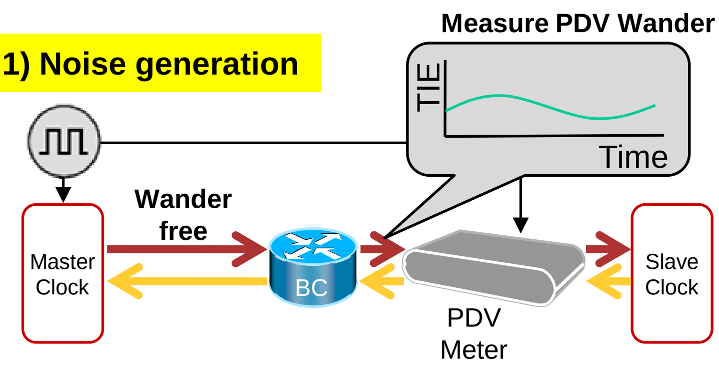
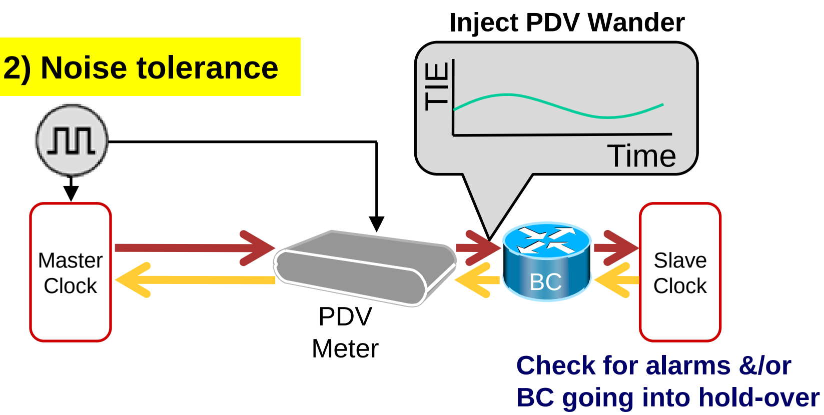
Boundary Clock Test Plan to G.8273.2

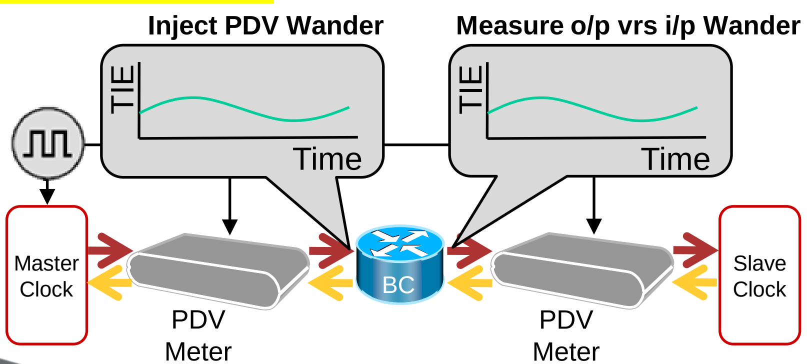
1) Noise generation



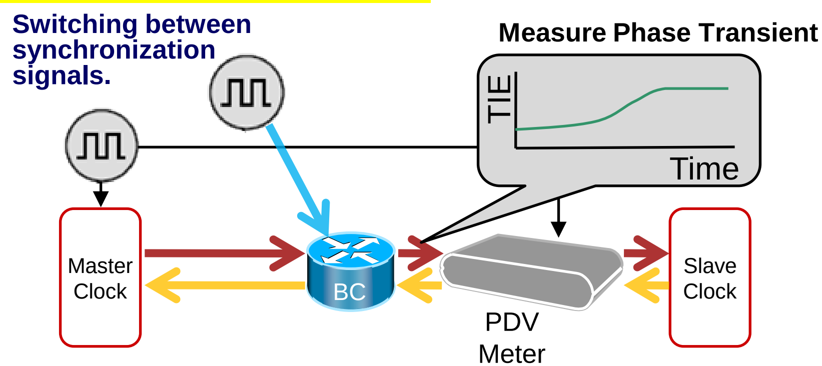
2) Noise tolerance



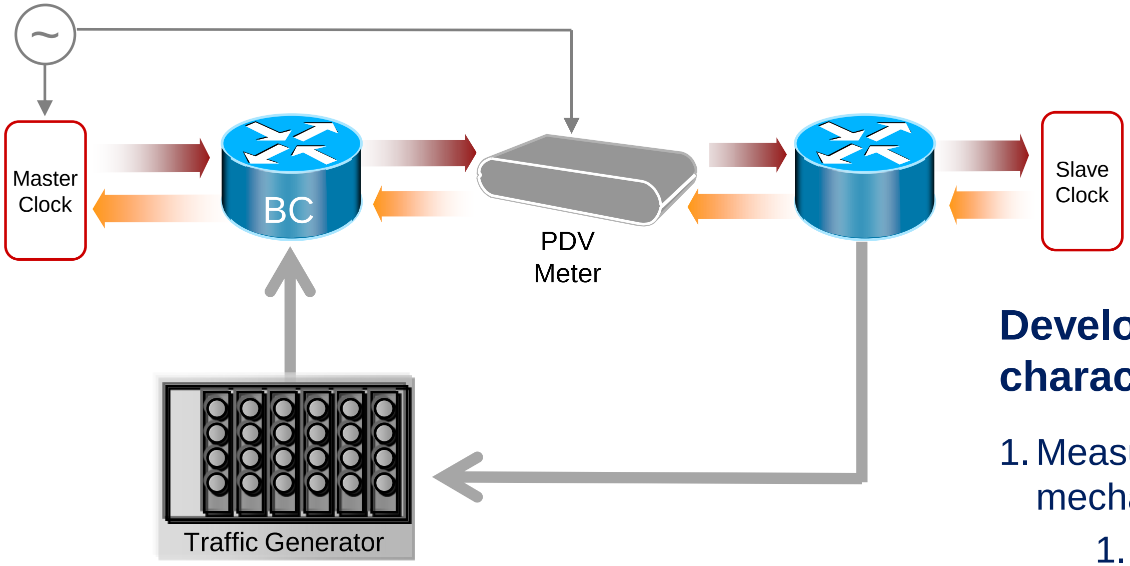
3) Noise transfer



4) Phase transient response



Boundary Clock Test Plan:
Impact of congestion traffic.



Congestion traffic e.g. conforming to
G.8261 VI.2.2 Network Traffic Model 2

Development Test Procedure to characterise actual performance

1. Measure PDV induced by policing and buffer mechanisms;
    1. Vary traffic packet size.
    2. Vary traffic priority.
    3. Vary traffic utilisation.
2. Test in 1-Step and 2-Step modes.

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Transparent Clocks

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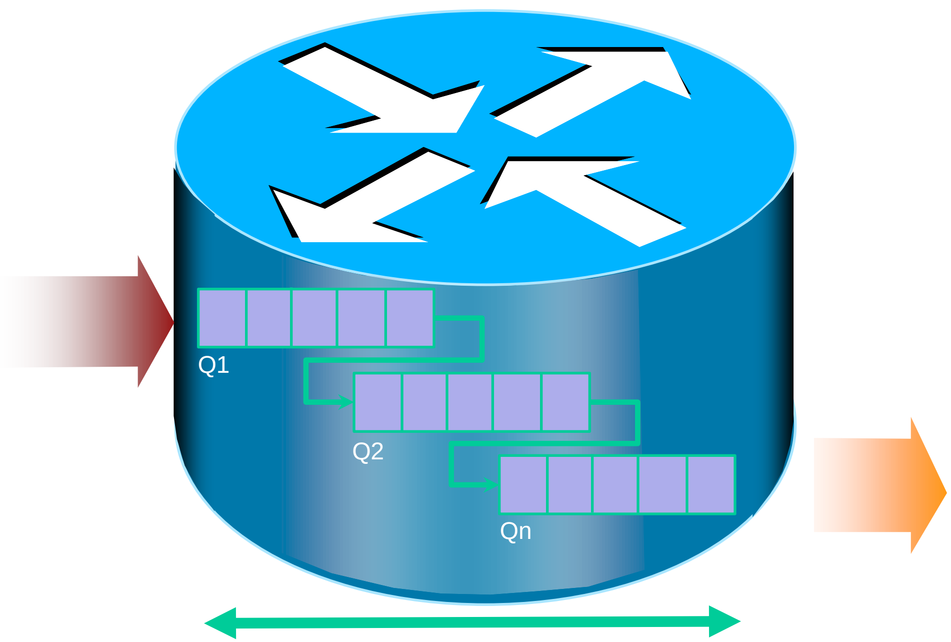
Transparent Clock



Packet Delay in TC Device
inserted into correctionField
at output of Transparent Clock device

Transparent Clocks reduce PDV by;

- Calculating the time a PTP packet resides in the TC device (in nsec) and insert the value into the correctionField.
- By using the correctionField, the Slave or terminating BC can effectively remove the PDV introduced by the TC.

PTP Message Header Format

Bits							
7	6	5	4	3	2	1	0
transportSpecific				messageType			
Reserved				versionPTP			
messageLength							
domainNumber							
Reserved							
Flags							
correctionField							
Reserved							

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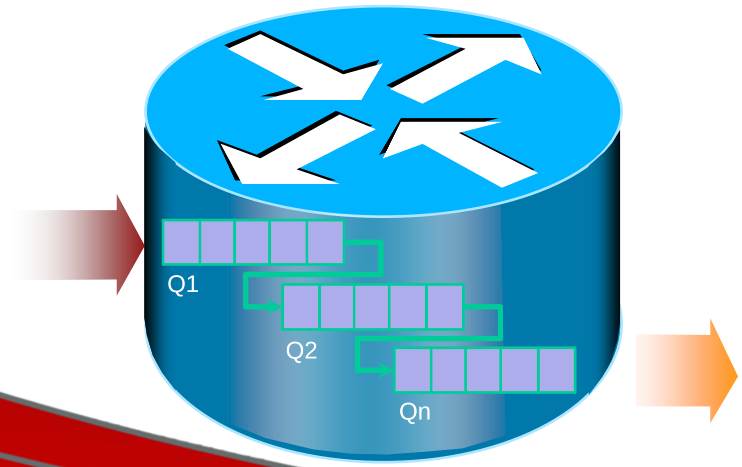
Accuracy of the Correctionfield value:
Does it reflect the actual delay experienced by the Sync & Del_Req messages?

Theoretical model:

- CorrectionField precisely reflects the delay through the equipment
- Ideal case **– zero net PDV**



Potential Sources of inaccuracy;

1. PDV introduced dependent on vendor's implementation;
   - Impact of **Output Buffer Queue** not removed.
     - 12 µsec for 1514 Byte packet, (G.8261).
     - 525 µsec for 64K Jumbo Byte packet
   - Varying sized Packets not corrected to same accuracy.
   - 1-step and 2-step processes produce different behaviour.
   - Does it make a difference if High Priority Traffic is present?
2. Is the TC correction effective in both directions?

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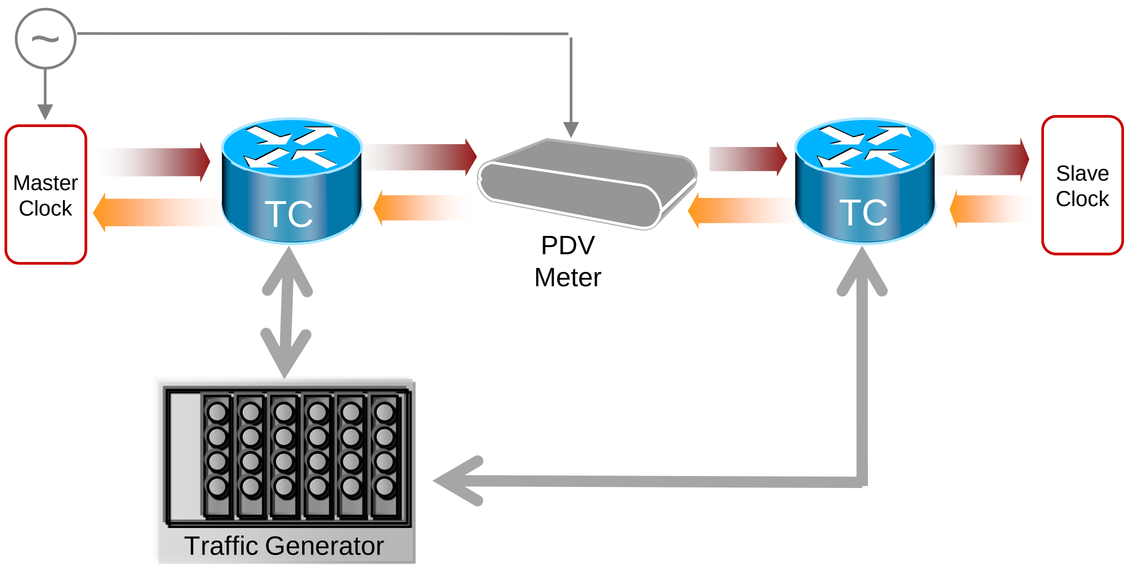
Transparent Clock Test Plan



Congestion traffic e.g.conforming to
G.8261 VI.2.2 Network Traffic Model 2

IEEE std C37.238-2011
PTP in Power Systems Applications.

- **Annex A:**
  TC TimeInaccuracy ≤50nsec.

Development Test Procedure to characterise actual performance

1. Measure impact of correctionField on Sync PDV.
    1. Vary traffic packet size.
    2. Vary traffic priority.
    3. Vary traffic utilisation.
2. Repeat for Del_req PDV.
3. Test in 1-Step and 2-Step modes.

- Run G.8261 Test case scripts and measure PDV with and without use of CorrectionField.
- For high accuracy measurement, measure PDV at input & output concurrently and calculate difference including the correctionField.

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Ordinary Clocks

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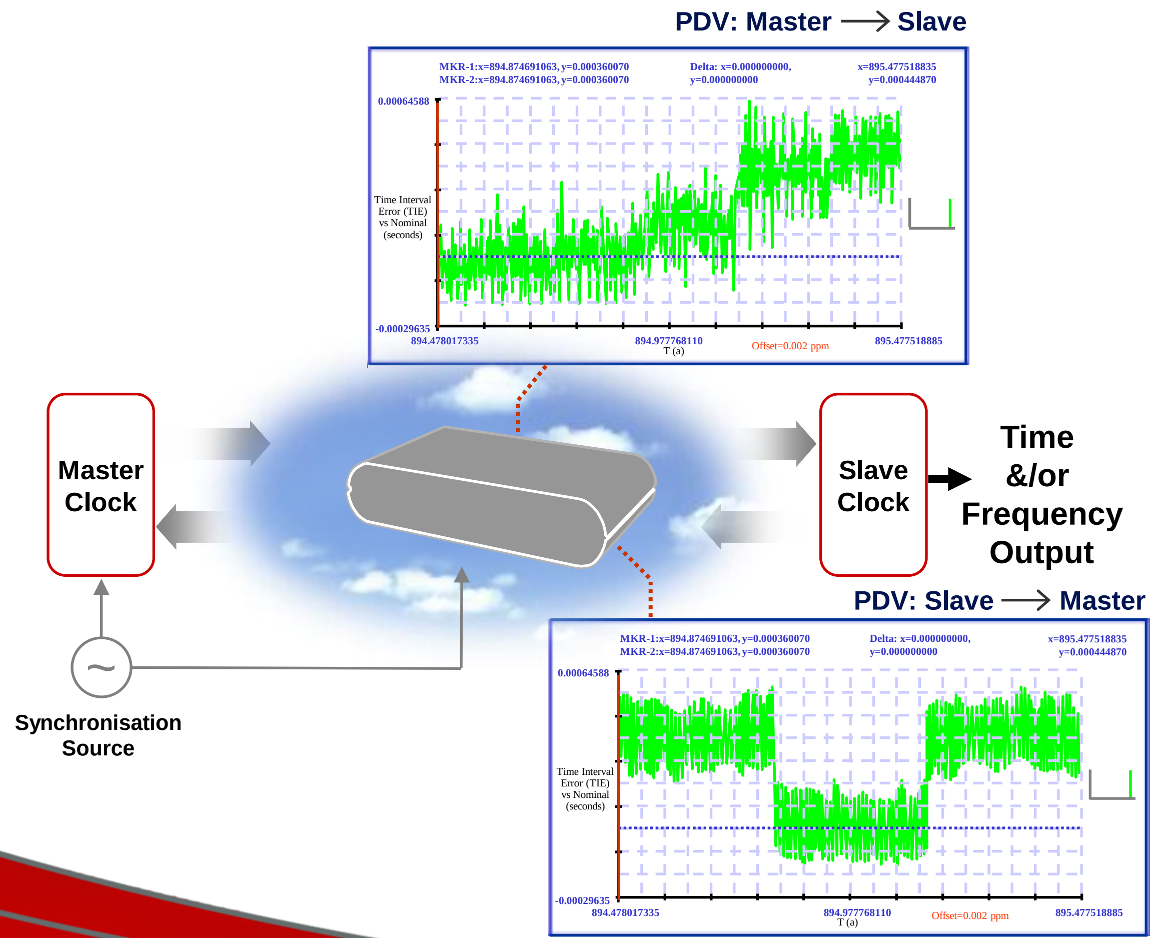
Prove performance in presence of congestion



- Congestion in both directions will impact clock recovery.
- **G.8261 Appendix VI** Test Cases are the most widely used approach to verifying operation.

Networks

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PDV Metrics

ITU-T G.8260: Appendix under development that defines a number of metrics that may be used for analysis of PDV.

- WD8260ND_G8260, WP3/15;
  ITU-T Recommendation G.8260 Latest Draft, York Sept.'11

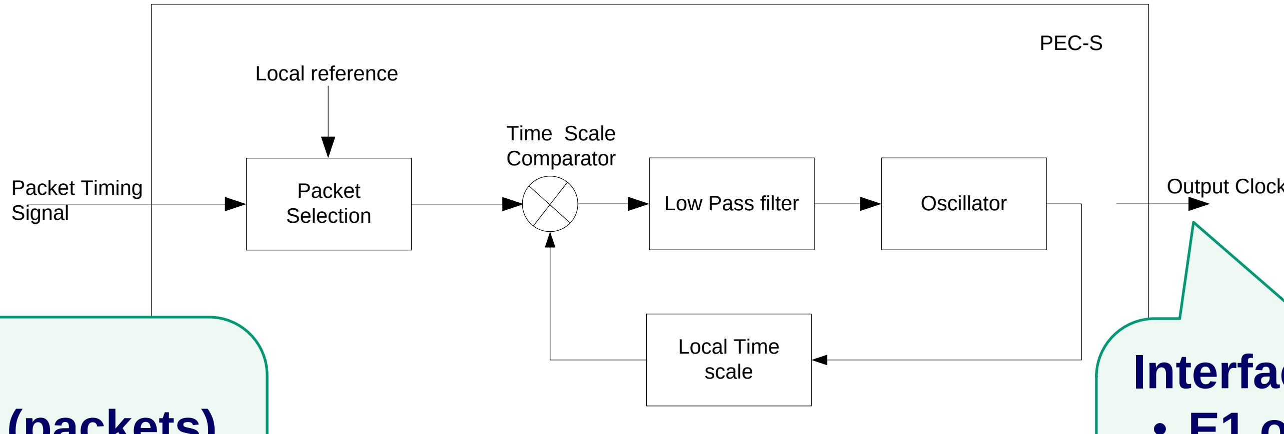
Metrics defined include;

- **MATIE , minMATIE -** Maximum Average Time Interval Error
- **MAFE, minMAFE -** Maximum Average Frequency Error
- **minTDEV, PercentileTDEV, BandTDEV** (TDEV – Time Deviation**)**
- **ClusterTDEV**
- **Floor delay packet population.**
- **pktfilteredTIE, pktfilteredMTIE, pktfilteredTDEV, pktfilteredFFO**

PDV Metrics

Objective: **Extract and identify the key characteristics of the PDV that impact the ability of the Slave to lock to the Master clock.**

Clock Block Diagram from ITU-T Standards



Interface:
- **Ethernet (packets)**

Metric:
- **pktfilteredMTIE, pktfilteredTDEV**

Interface:
- **E1 or T1**

Metric:
- **MTIE, TDEV**

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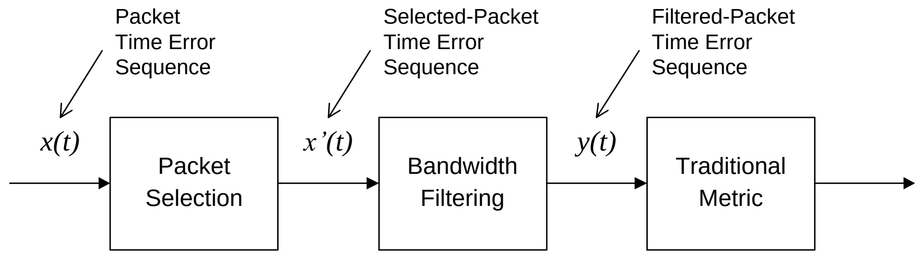
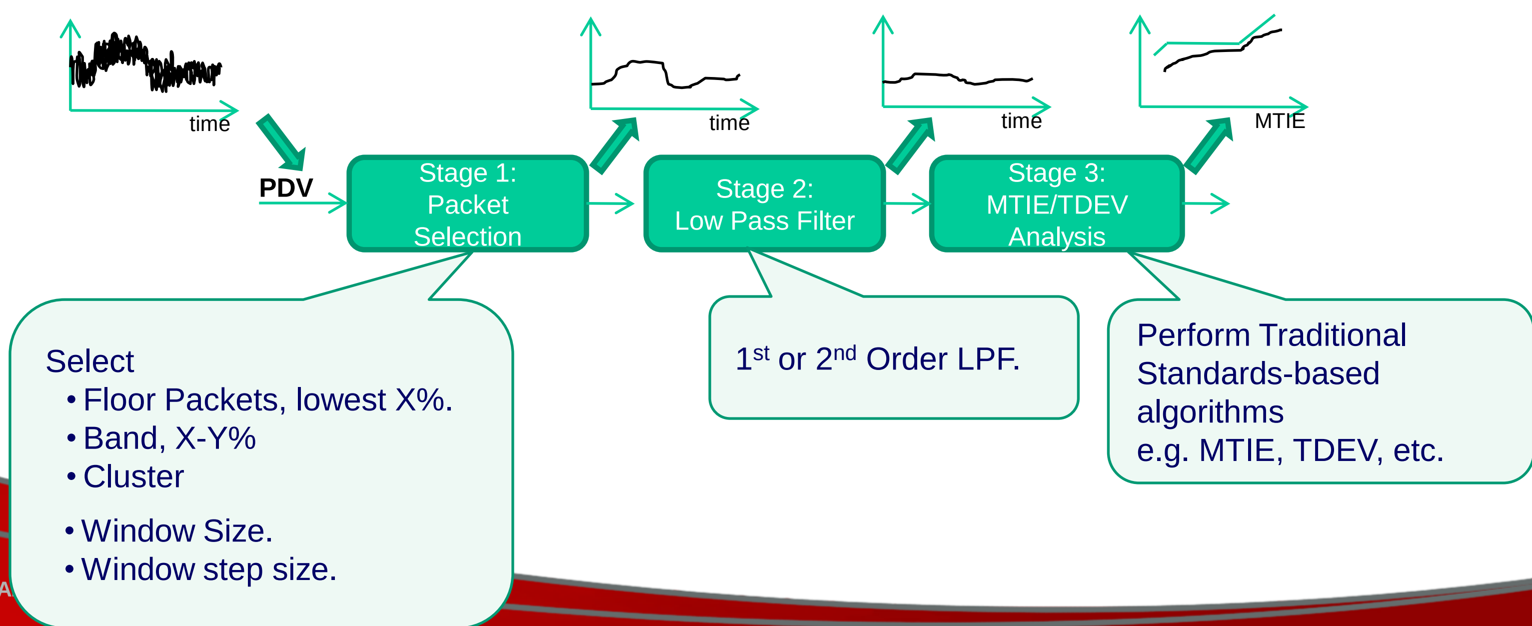
PDV pktfiltered Metrics



G.8260 Figure X - Packet selection & Filtering Flow



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Summary of Evaluation Plan

- **SyncE**
- **1588v2**
  - **BC**
  - **TC**
  - **Ordinary Clocks**
  - **Networks**

SyncE:
- Standards in force.
- G.8262
  - Wander
  - Jitter
- G.8264
  - ESMC behaviour

BC:
- G.8273.2 Standard under development.
  - Noise Generation
  - Noise Tolerance
  - Noise Transfer
  - Phase Transient & Holdover;
- Consider behaviour during Traffic Congestion.

TC:
- Prove accuracy of CorrectionField.
  - Characterise specific TC behaviour.
- IEEE Std C37.238-2011 'PTP in Power Systems Applications'
  - Profile specify ≤50nsec.

Ordinary Clocks:
- Character using G.8261 Appendix VI test cases.
- A number of metrics under development in Draft Appendix in G.8260.

Networks:
- A number of metrics under development in Draft Appendix in G.8260.
  - pktfilteredMTIE, pktfilteredTDEV
  - MAFE, minTDEV, etc

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Calnex Paragon Sync

- IEEE 1588v2
- CES
- Sync-E
- OAM