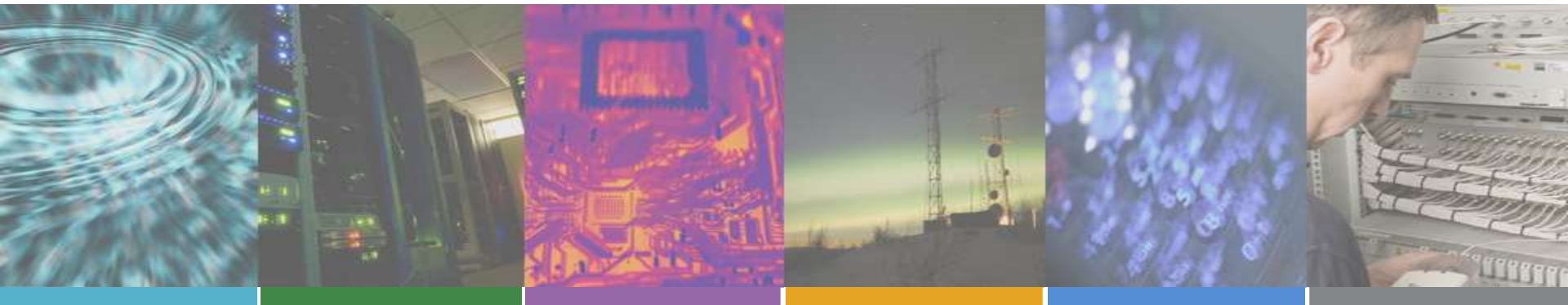


Tutorial: Network-based Frequency, Time & Phase Distribution



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5th Nov 2013

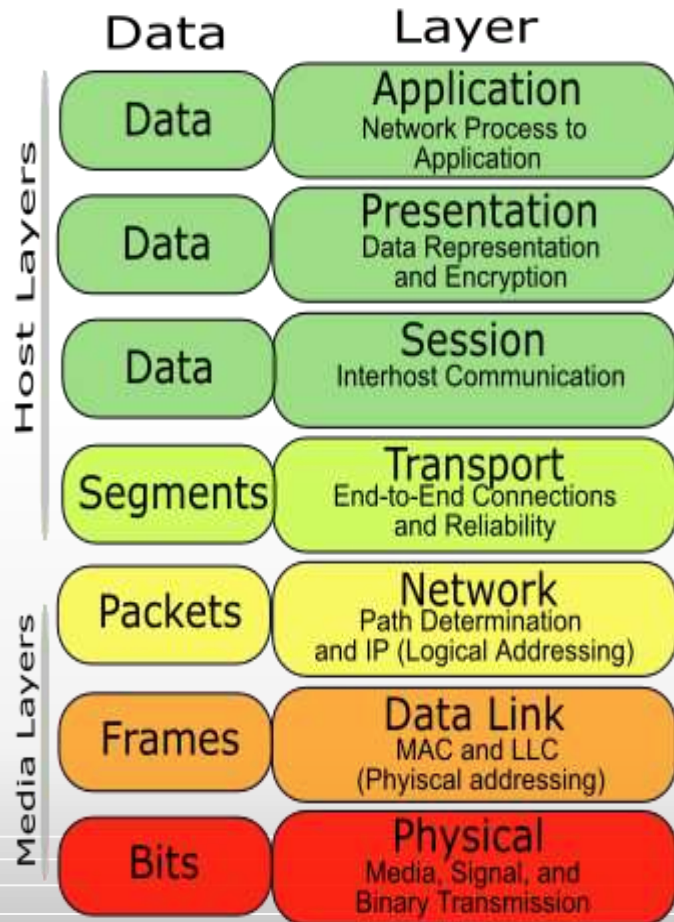
ITSF – Lisbon

Presentation Contents

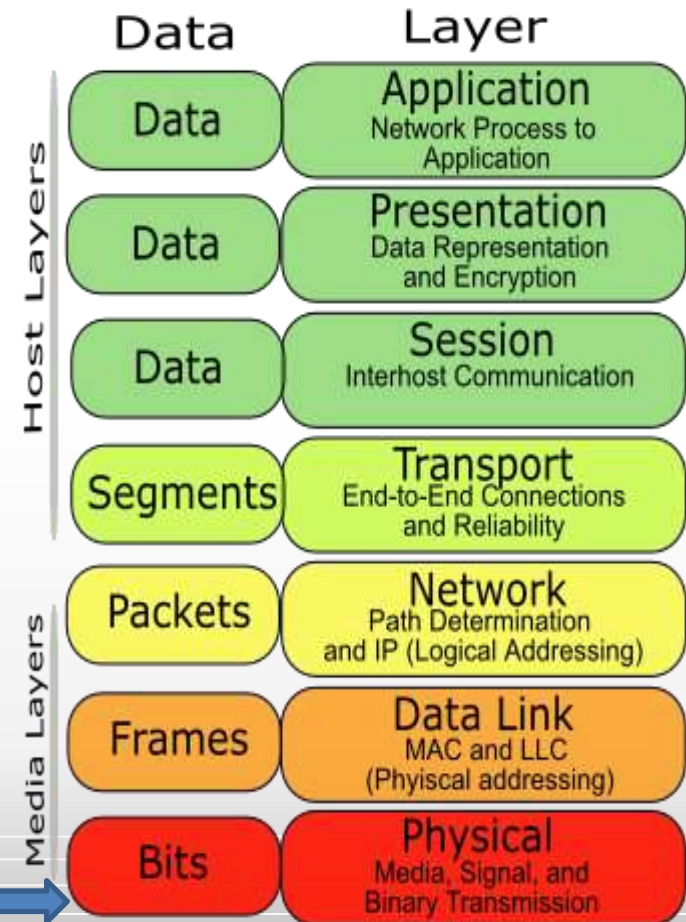
- Introduction
- Physical Layer Distribution
- Packet Layer Distribution
- Summary

The (in)famous stack model

OSI Model

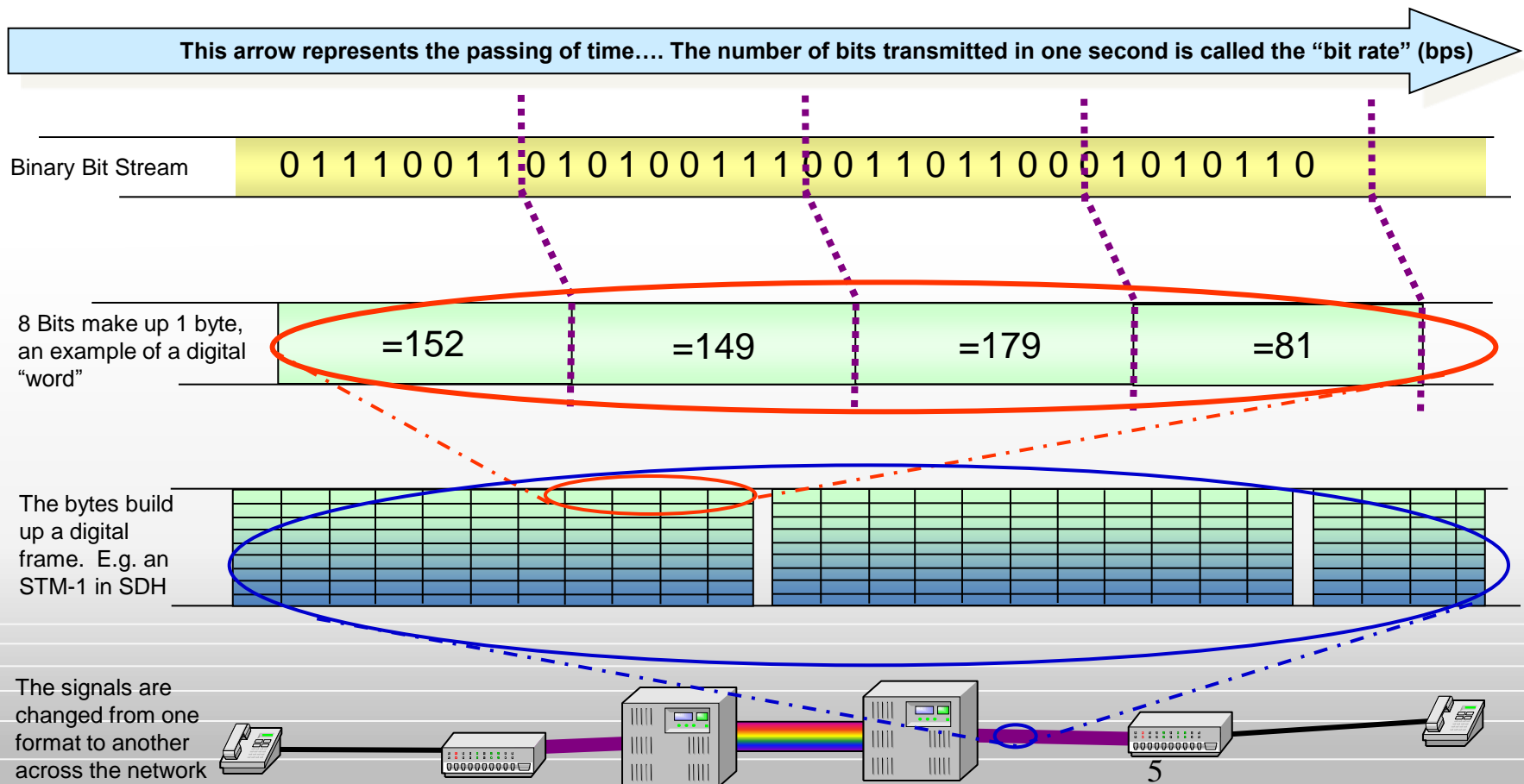


OSI Model



Bits and Bytes

- Digital signals are transmitted as a stream of single “Bits”. A Digital Bit is the underlying base of all digital communications, its value can either be a binary “0” or a “1”, the “0”s and “1”s are used to build digital “words” and ultimately make up all digital services.

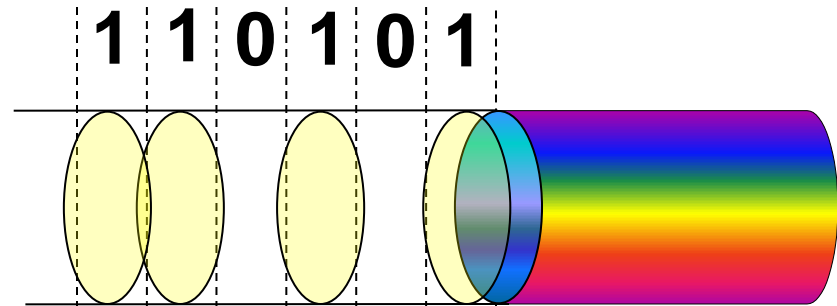


How Are “Bits” Represented..?

- The value of a Bit (0 or 1) can be represented by different modulations of a carrier signal examples are:

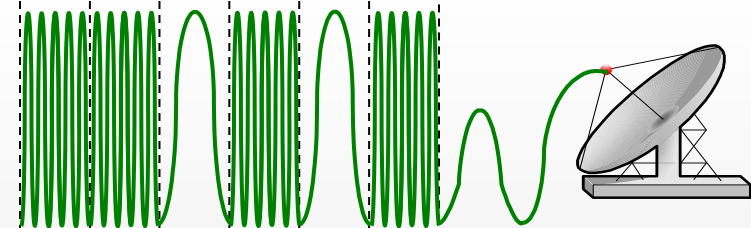
- Fibre Optics

- The presence or absence of a light pulse
- Different frequencies of light



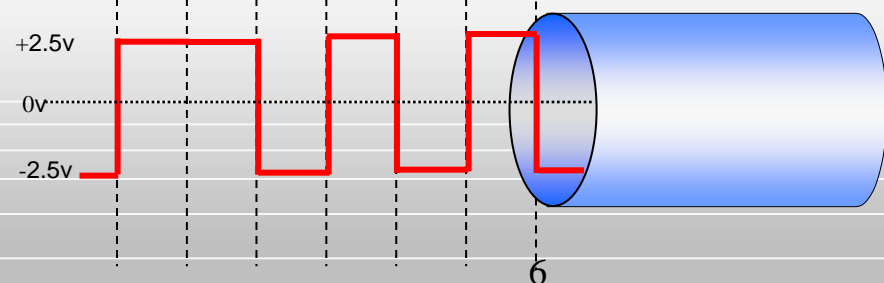
- Radio/Microwaves - Mobile phone, satellite comms, WiFi, etc.

- Changes in phase, frequency or amplitude of the electromagnetic waves



- Electrical Cabling - Coaxial, twisted pair, etc

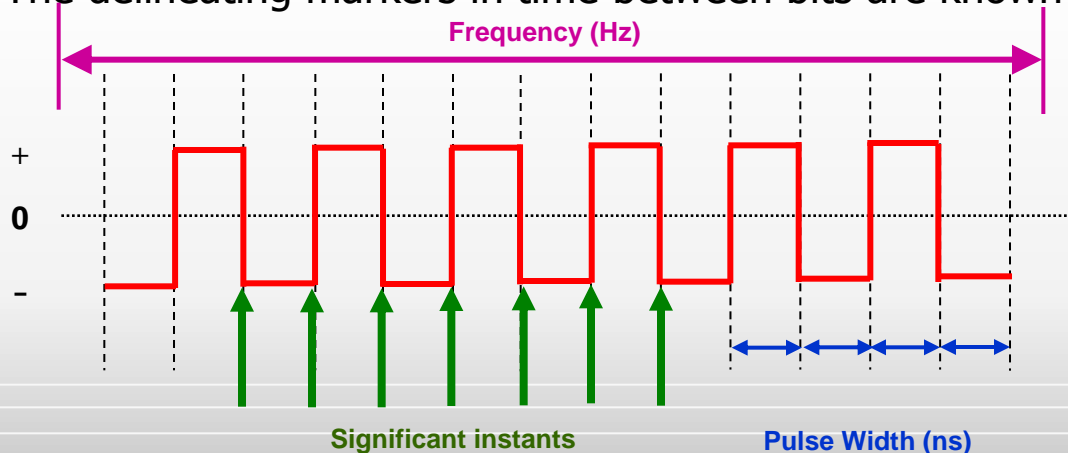
- Voltage levels on the wire



The bits arrive at regular intervals, represented here

Timing (Frequency) Signal Characteristics

- **Frequency** - *noun*. - the number of periods or regularly occurring events of any given kind in unit of time. dictionary.com
- The intervals between the bits is known as the "pulse width" and is directly related to the bitrate of the signal. These are usually measured in nanoseconds (ns).
- The faster the bitrate, the shorter the pulse width.
- The frequency of a signal refers to the number of "cycles" per second and is measured in Hertz for an analogue signal with no digital data mapped onto it or bits per second (bps) for a digital data signal.
- The delineating markers in time between bits are known as "significant instants"



Pulse Width = 1/Frequency

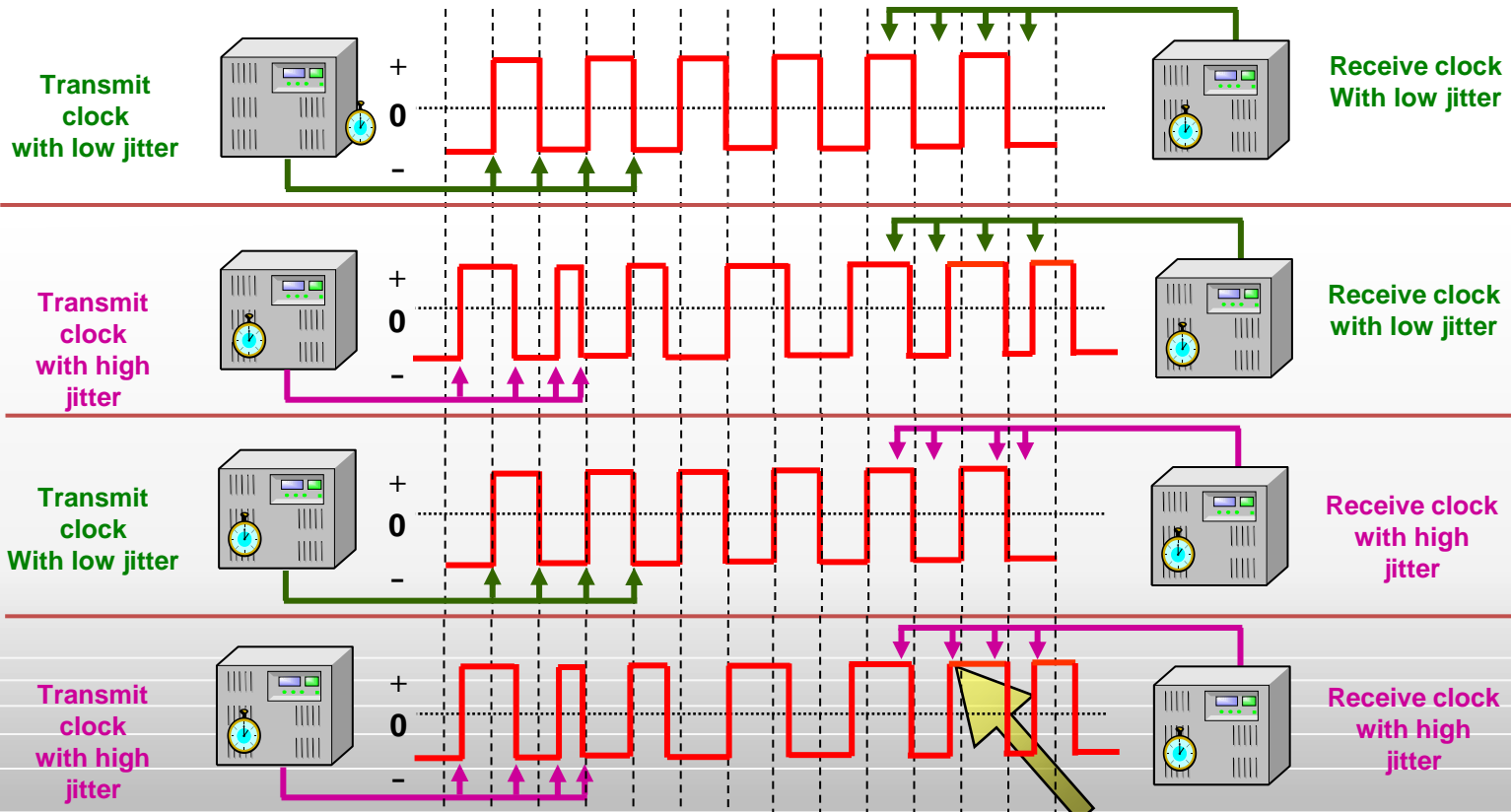
For an E1 signal:

$1 / 2.048 \text{ Mbps}$
 $= 1 / 2048000 \text{ bps}$
 $= 0.00000048828125 \text{ s}$
 $= 488.28 \text{ ns}$

TIME

Bit Synchronisation

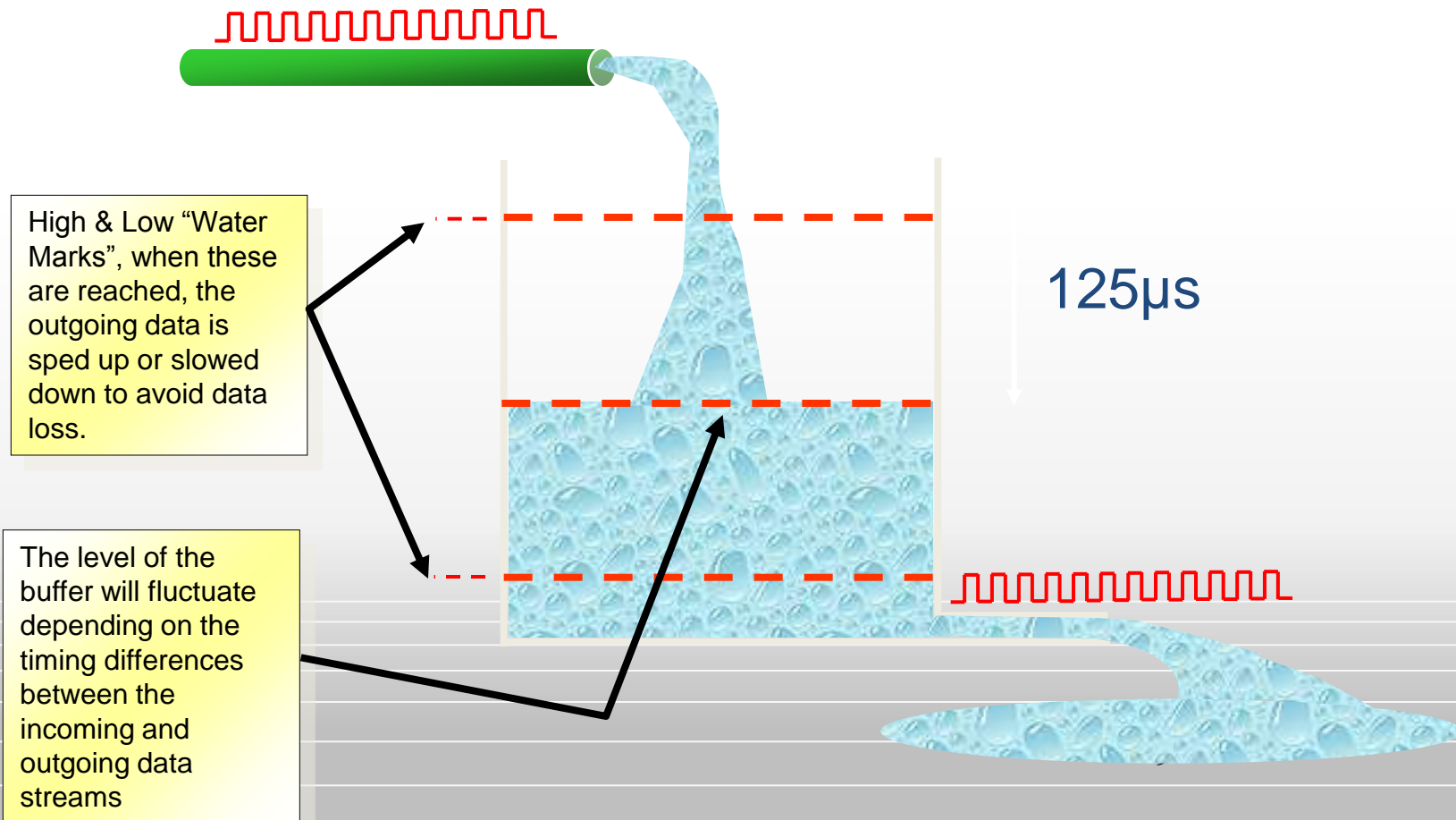
- The precise frequency and pulse width of a transmitted signal are determined by a clock on the network equipment, the "Write Clock"
- Receiving equipment has a "Read Clock" that determines the precise time that the received signal is sampled.
- The clocks of the two elements must be within set tolerances or the signal may be misread.



Is this bit a "0" or a "1" ???

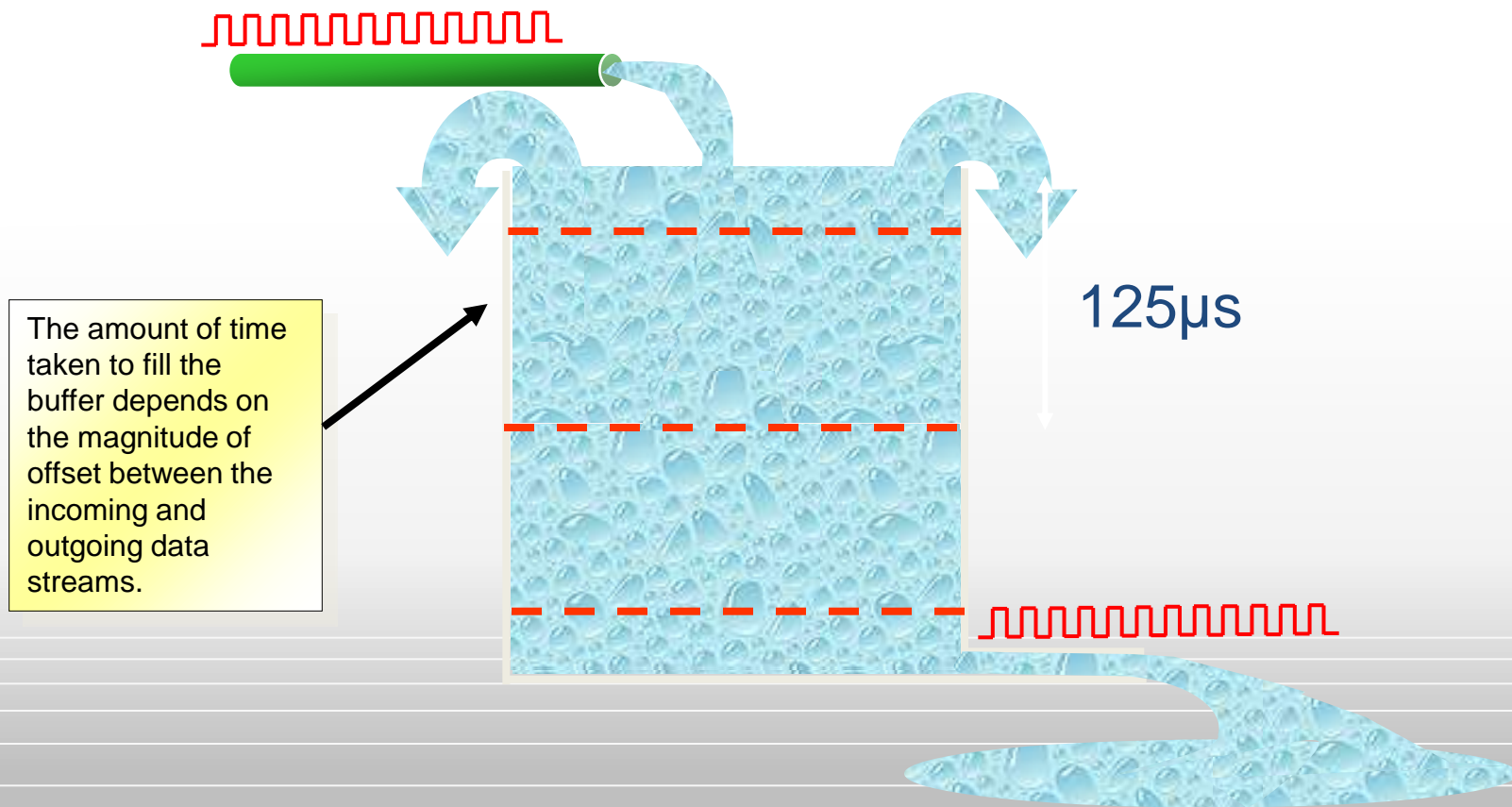
The FIFO Buffer

- The First In First Out buffer is a store where the incoming data stream is temporarily held prior to processing.
- A common buffer size in SDH is $2 \times 125\mu\text{s}$, this is exactly two E1 frames.
- The buffer cannot be too large it adds delay in the transmission



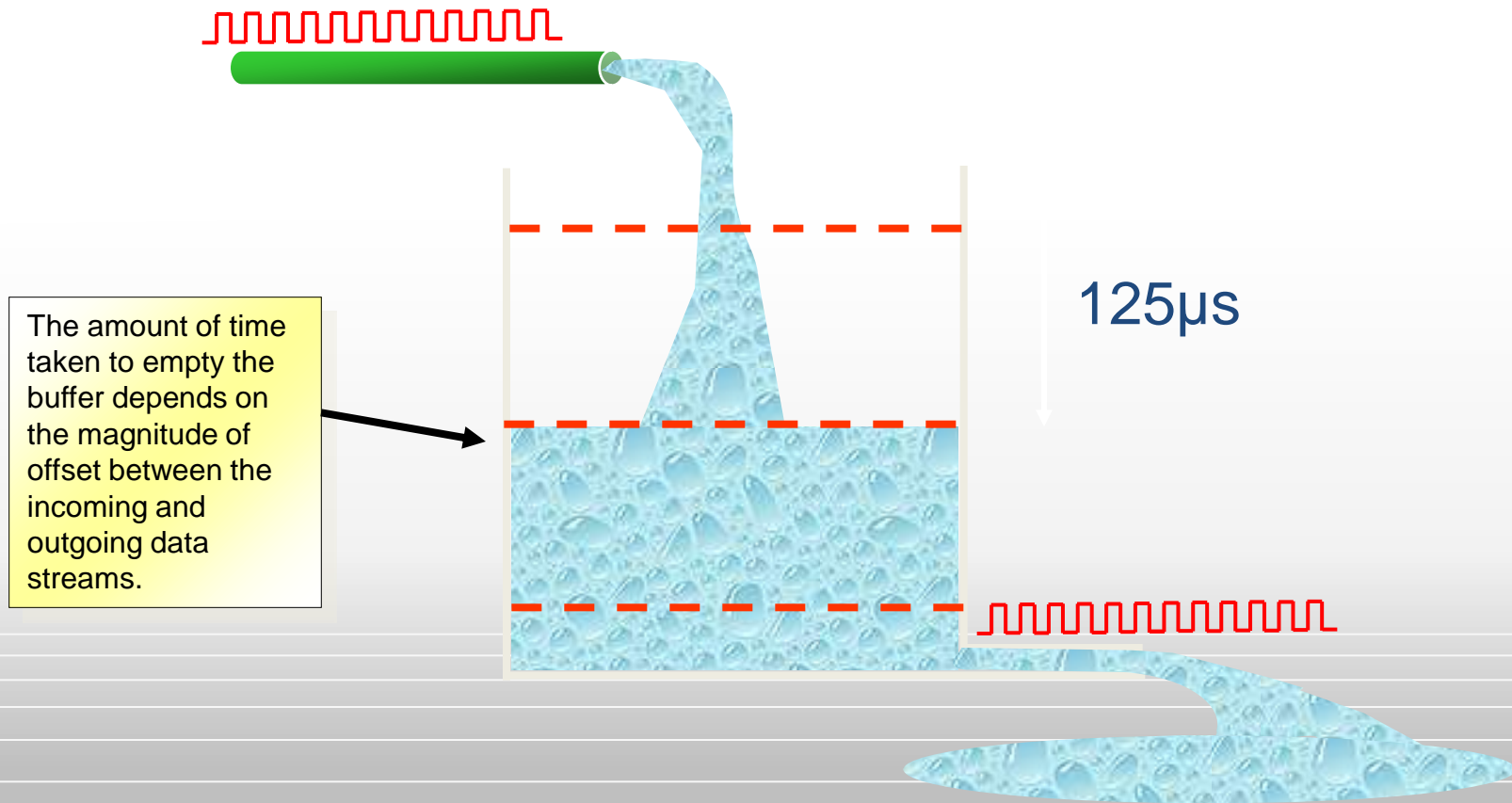
The FIFO Buffer – Sending too fast

- If the data is being received at a faster rate than it is being sent then the buffer begins to fill.
- Once the buffer has no more room for any more data a whole 125 μ s frame of data is lost.



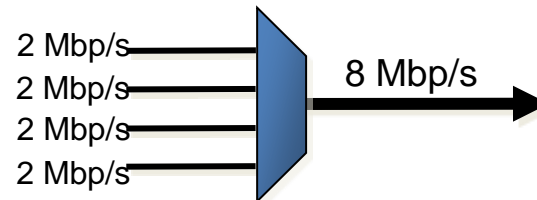
The FIFO Buffer – Sending too slow

- If the data is not received fast enough then the buffer will empty.
- As the equipment will have nothing to send, usually the last full frame received will be repeated.
- This maintains communications on the outgoing channel but the data is useless.

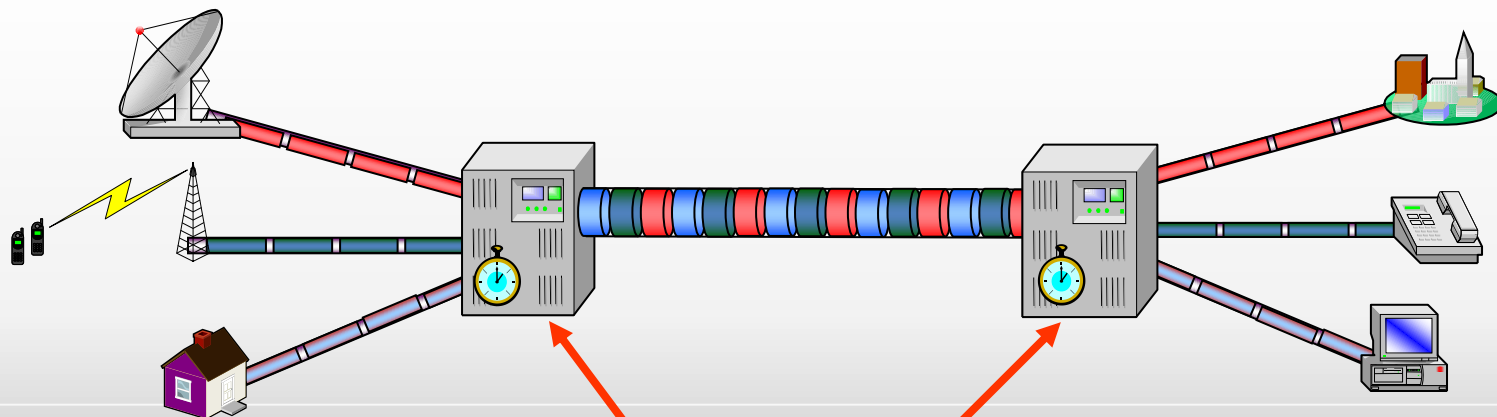


Time Division Multiplexing (TDM)

- Multiplexing is the method of combining two or more lower rate signals into a single higher rate signal for transport over a single transmission medium.



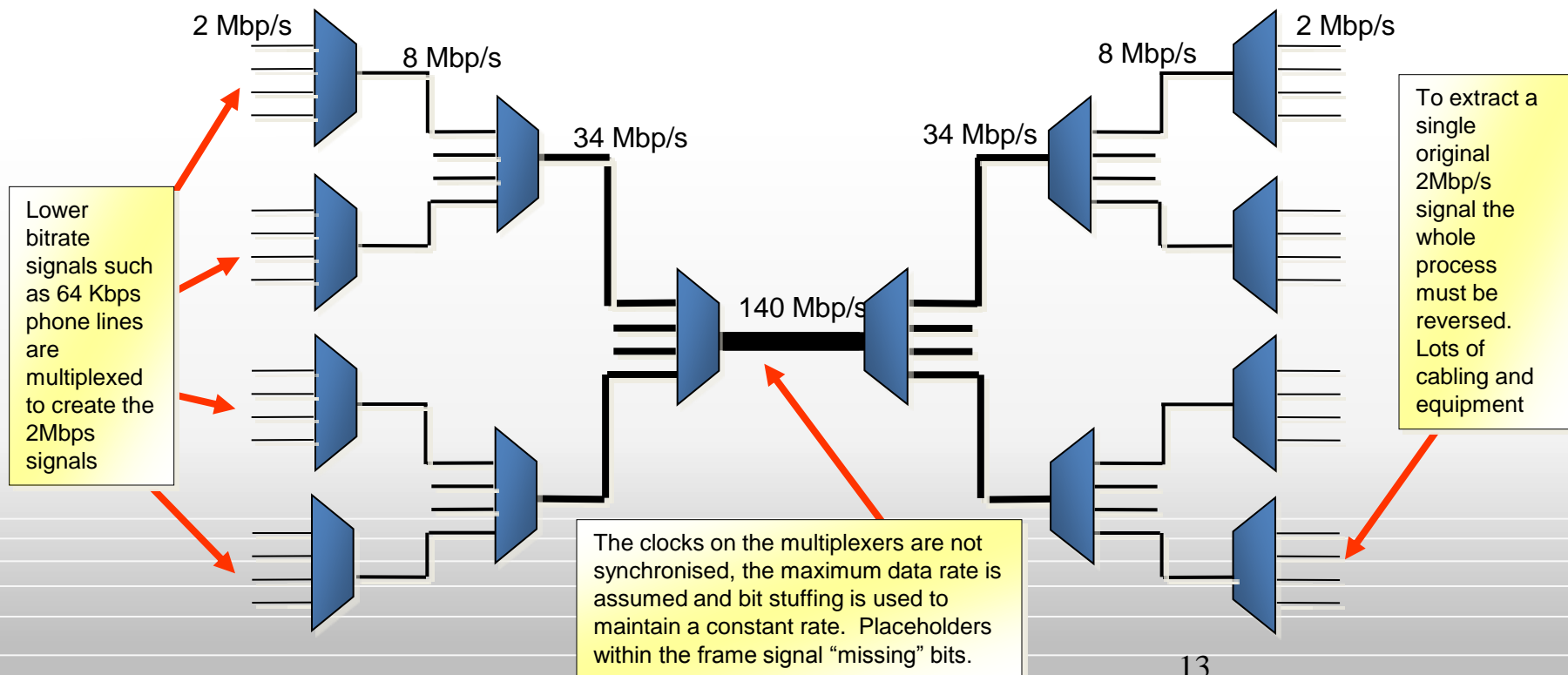
- Data is transmitted in chunks usually referred to as bytes, cells or frames.
- The frames each have a "timeslot" reserved in the higher rate signal.



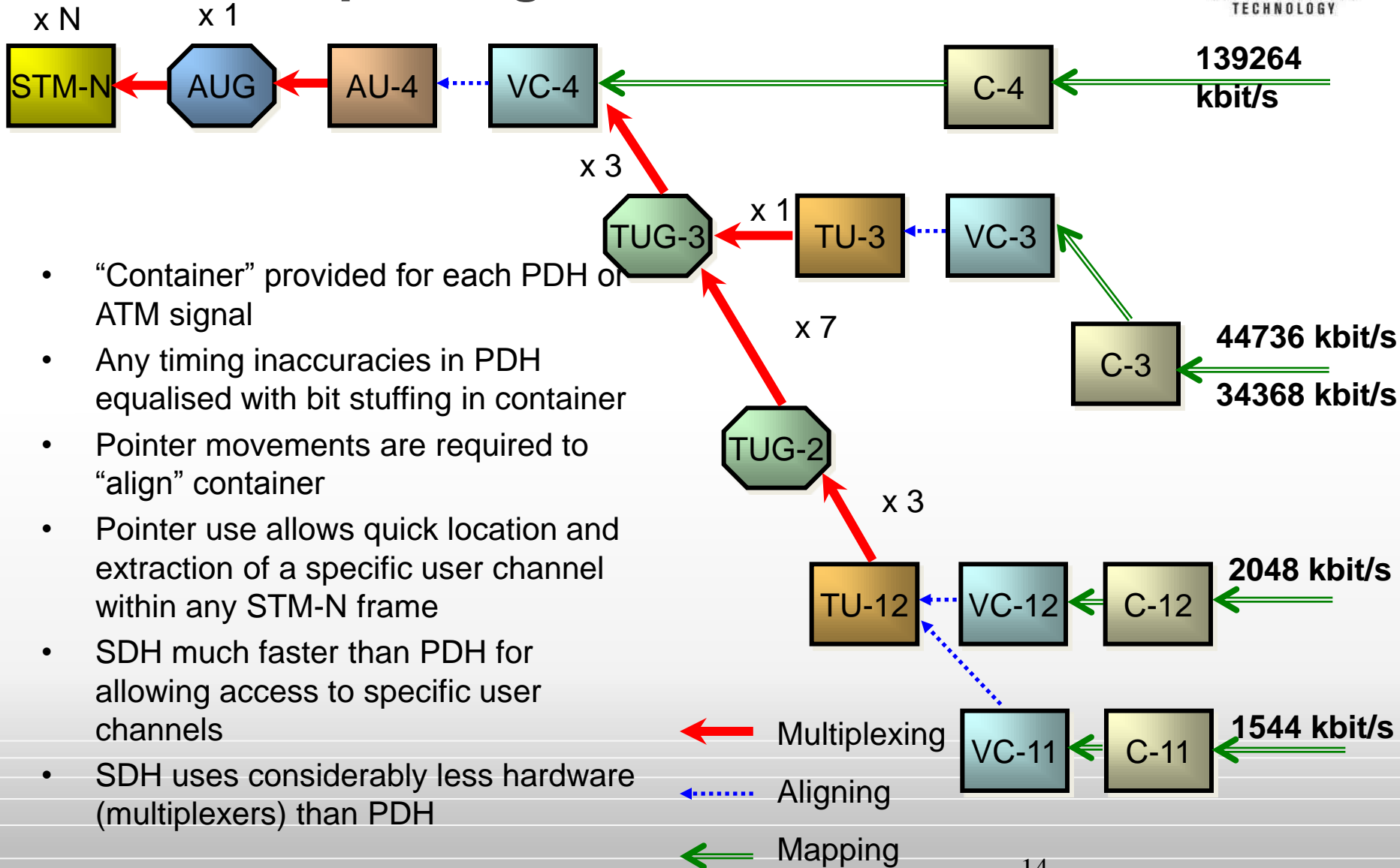
The clocks on the multiplexers / de-multiplexers must be synchronised to allow correct differentiation between frames and a smooth flow of data

PDH Multiplexing

- Plesiochronous Digital Hierarchy is a method of multiplexing signals into higher rates then de-multiplexing when required.
- Plesiochronous - "pleasi" – near and "chronos" – time. The clocks on the equipment run at a nominal frequency within a set tolerance, any frequency offsets are taken up by "bit stuffing", the addition of extra bits to fill the transmission.



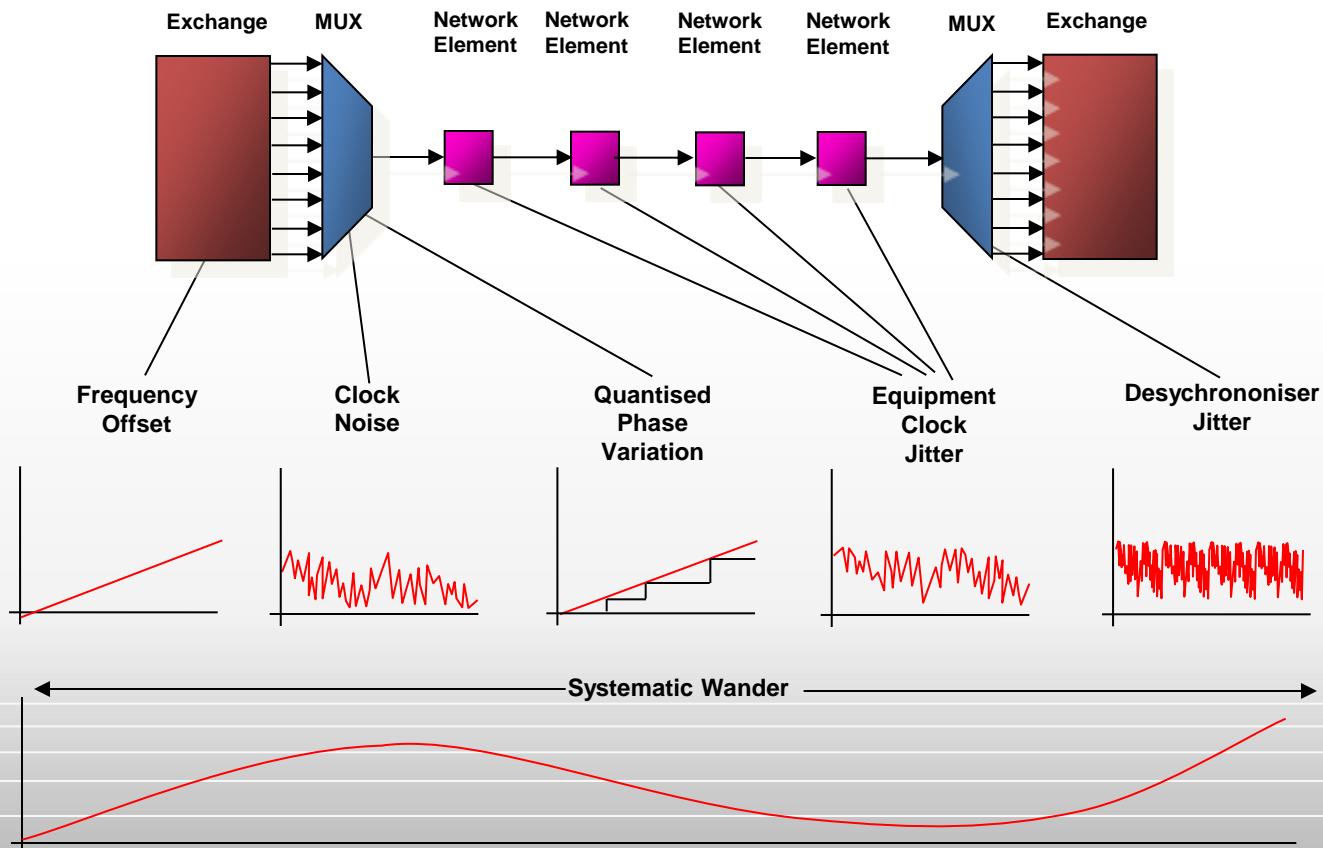
SDH Multiplexing



- “Container” provided for each PDH or ATM signal
- Any timing inaccuracies in PDH equalised with bit stuffing in container
- Pointer movements are required to “align” container
- Pointer use allows quick location and extraction of a specific user channel within any STM-N frame
- SDH much faster than PDH for allowing access to specific user channels
- SDH uses considerably less hardware (multiplexers) than PDH

Noise Accumulation

- As a synchronisation is passed through network elements, additional noise is accumulated along the sync trail.



Sync Trail Architecture Rules



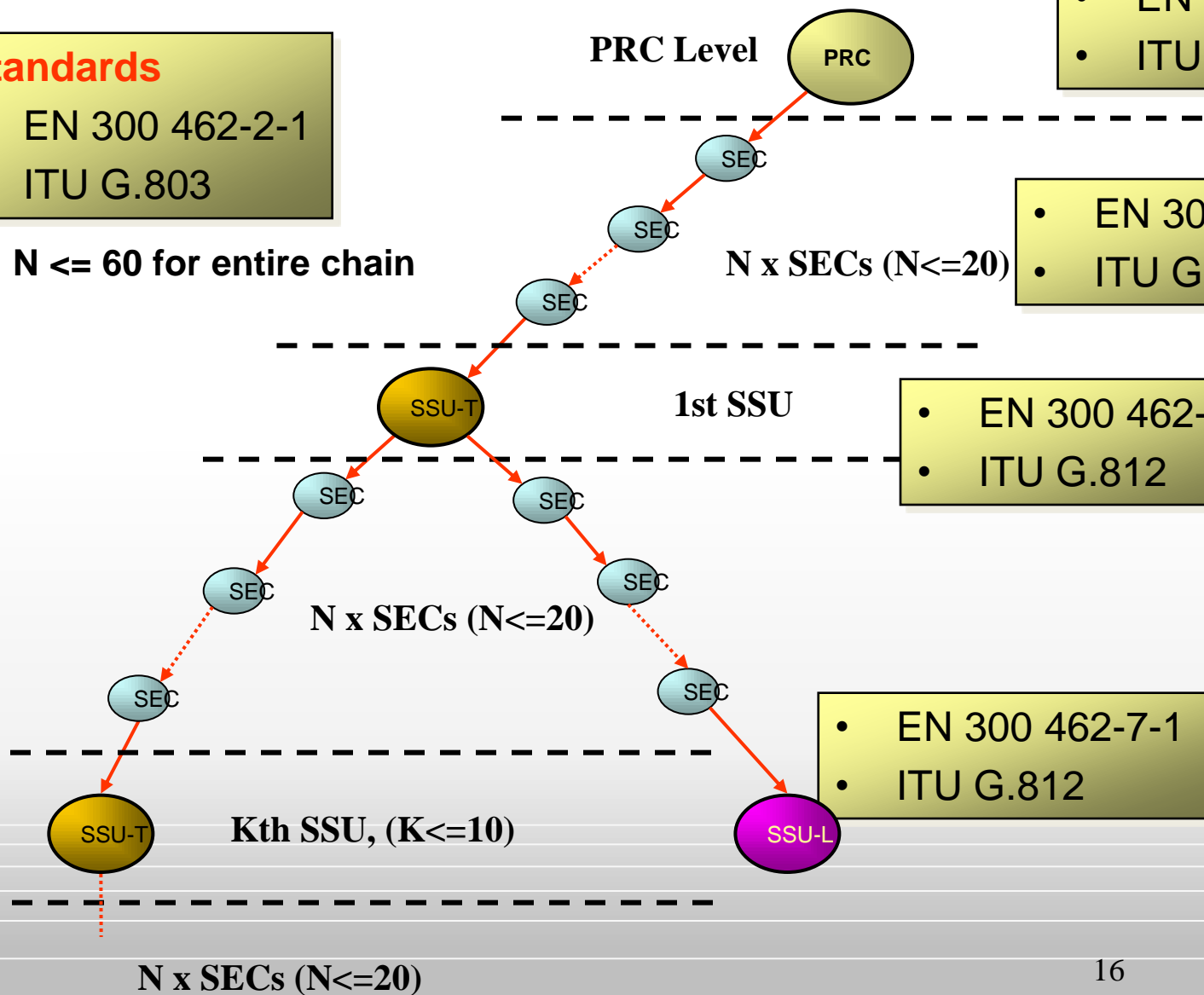
- Standards**
- EN 300 462-2-1
 - ITU G.803

- EN 300 462-6-1
- ITU G.811

- EN 300 462-5-1
- ITU G.813

- EN 300 462-4-1
- ITU G.812

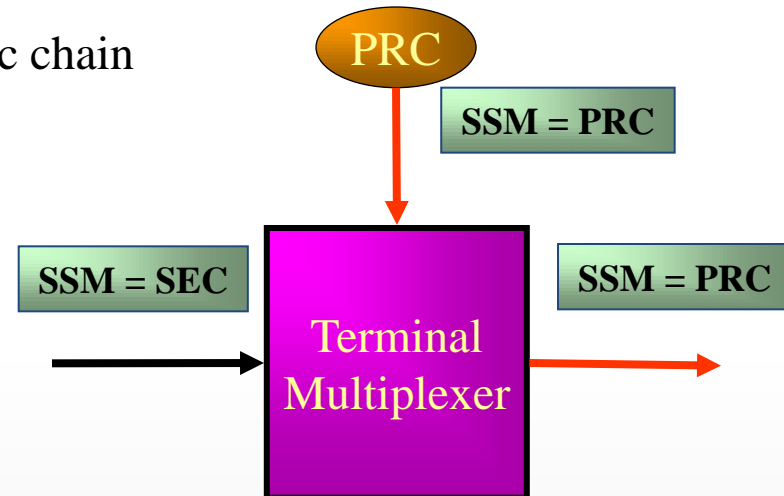
- EN 300 462-7-1
- ITU G.812



N x SECs (N<=20)

Synchronisation Status Message in SDH

- SSM in Bits 5-8 of S1 byte of STM-N G.707
- SSM is a quality indicator for the source of the sync chain
 - Defined in EN 300 417-6-1
- Always select best clock input in selection list
 - $SSM_{out} = SSM_{in}$ of selected source
- SSM overrides operator priority selection
- Assumed quality assigned to non SSM supporting interfaces



S1 Byte (bits 5-8)	Source of Sync Trail
0000	Synchronisation quality unknown
0010	PRC - EN 300 462-6-1
0100	SSU-T - EN 300 462-4-1
1000	SSU-L - EN 300 462-7-1
1011	SEC (SETS) - EN 300 462-5-1
1111	Do Not Use (DNU) for synchronisation

Standards

- G.707
- EN 300 147
- EN 300 417-6-1

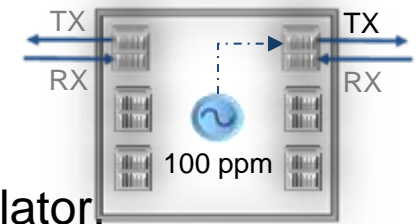
SyncE Overview



How is SyncE different from normal Ethernet?

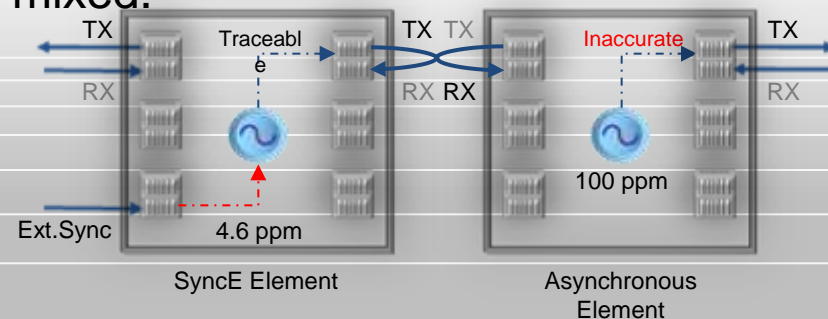
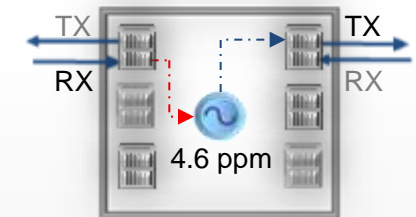
Existing Ethernet PHY (Physical Layer)

- IEEE 802.3 defines Ethernet PHY
- Rx uses incoming line timing. Tx uses free-running 100ppm oscillator.
- No relationship between the Rx & Tx.

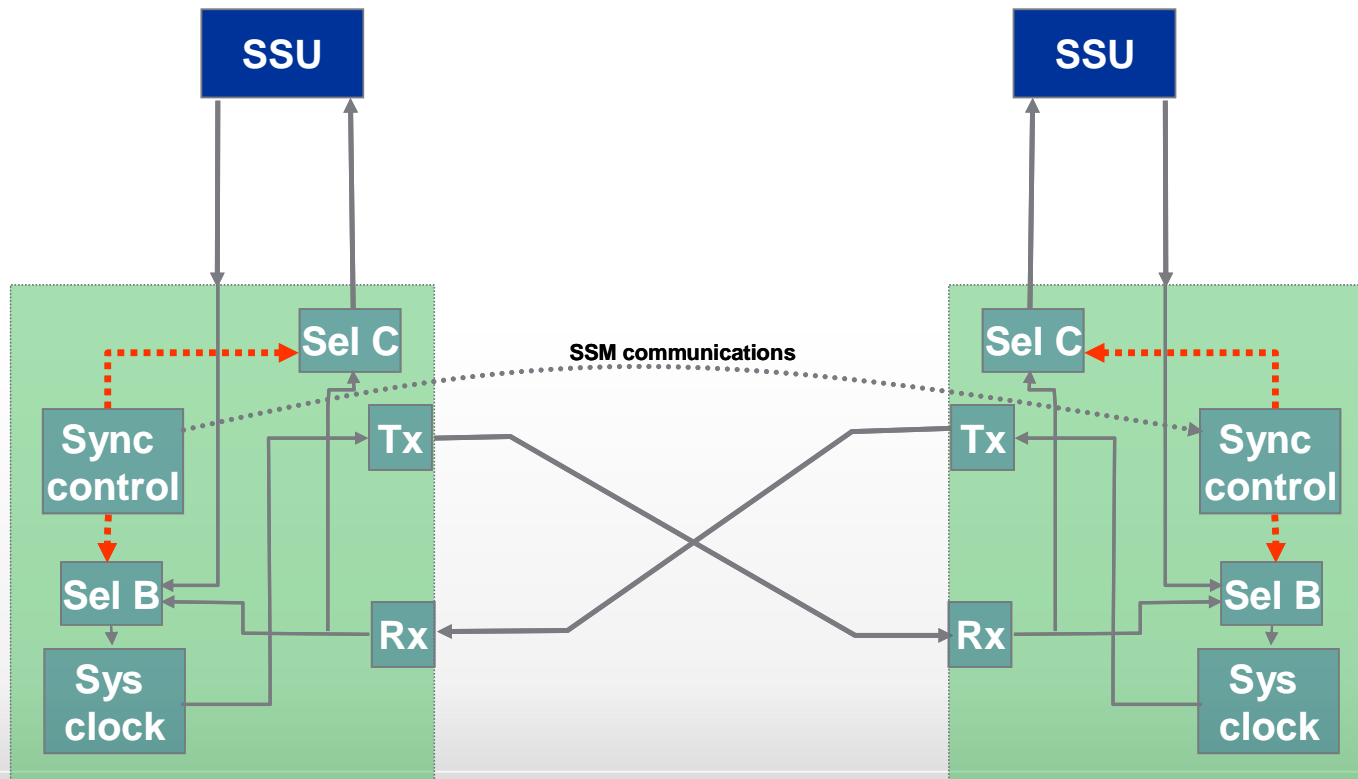


SyncE PHY (Physical Layer)

- Rx disciplines the internal oscillator
- Tx uses the traceable clock reference, creating end-to-end scheme.
- PRC can provide the reference. SSUs filter jitter/wander.
- SyncE and asynchronous switches **cannot** be mixed.



QL in SyncE - ESMC



ESMC PDU format

Octet number	Size/bits	Field
1-6	6 octets	Destination Address = 01-80-C2-00-00-02 (hex)
7-12	6 octets	Source Address
13-14	2 octets	Slow Protocol Ethertype = 88-09 (hex)
15	1 octet	Slow Protocol Subtype = 0A (hex)
16-18	3 octets	ITU-OUI = 00-19-A7 (hex)
19-20	2 octets	ITU Subtype
21	bits 7:4 (Note 1)	Version
	bit 3	Event flag
	bits 2:0 (Note 2)	Reserved
22-24	3 octets	Reserved
25-1532	36-1490 octets	Data and padding (See point j)
Last 4	4 octets	FCS

NOTE 1 – Bit 7 is the most significant bit of octet 21. Bit 7 to bit 4 (bits 7:4) represent the four-bit version number for the ESMC.

NOTE 2 – The three least significant bits (bits 2:0) are reserved.

QL TLV format

Standards

- G.8264

Octet number	Size/bits	Field
1	8 bits	Type: 0x01
2-3	16 bits	Length: 00-04
4	bits 7:4 (Note)	0x0 (unused)
	bits 3:0	SSM code

NOTE – Bit 7 of octet 4 is the most significant bit. The least significant nibble, bit 3 to bit 0 (bits 3:0) contain the four-bit SSM code.

ESMC & IEEE 802.3ay OSSP



esmc.pcap [Wireshark 1.8.3 (SVN Rev 45256 from /trunk-1.8)]

File Edit View Go Capture Analyze Statistics Telephony Tools Internals Help

Filter: Expression... Clear Apply Save IQ tfr b/cast from probe

No.	Time	Source	Destination	Protocol	Length	Info
1	0.000000	00:00:00_00:00:2b	slow-Protocols	ESMC	60	Event:Information, QL-PRC

Frame 1: 60 bytes on wire (480 bits), 60 bytes captured (480 bits)

- Ethernet II, Src: 00:00:00_00:00:2b (00:00:00:00:00:2b), Dst: slow-Protocols (01:80:c2:00:00:02)
 - Destination: slow-Protocols (01:80:c2:00:00:02)
 - Source: 00:00:00_00:00:2b (00:00:00:00:00:2b)
 - Type: Slow Protocols (0x8809)
- Organization specific slow Protocol
 - Slow Protocols subtype: organization specific slow Protocol (0x0a)
 - OUI: 0019a7 (Itu-T)
 - ITU-T OSSP Subtype: 0x0001: ESMC, Event:Information, QL-PRC
 - 0001 = Version: 0x01
 - 0... = Event Flag: Information ESMC PDU (0x00)
 -0.. = Timestamp Valid Flag: Not set. Do not use Timestamp value even if Timestamp TLV present (0x00)
 - Reserved: 0x00000000
 - ESMC TLV, QL-PRC
 - TLV Type: Quality Level (0x01)
 - TLV Length: 0x0004
 - 0000 = Unused: 0x00
 - 0010 = SSM Code: QL-PRC, Primary reference clock (G.811) (0x02)
 - Padding: 00..., 32 octets

```
0000 01 80 c2 00 00 02 00 00 00 00 00 2b 88 09 0a 00
0010 19 a7 00 01 10 00 00 00 01 00 04 02 00 00 00 00
0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030 00 00 00 00 00 00 00 00 00 00 00 00
```

Frame (frame), 60 bytes Packets: 1 Displa... Profile: Default

From clocks to packets

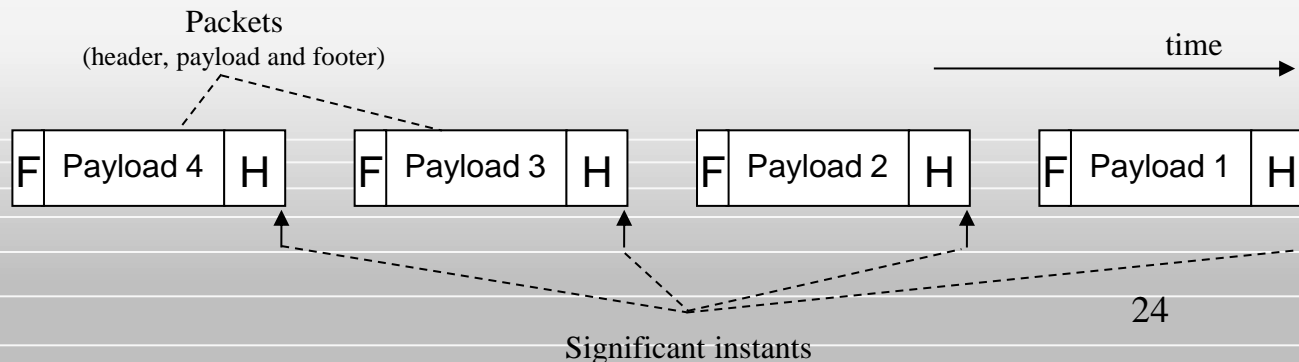
- It's just transfer of information...
 - A detectable event signifies the passage of a certain amount of time:
Clock Chimes... Ticks... Clock Edges...



- Analogue clock signals – known transmission media – known delays etc.
- By their very nature packet transmission systems have indeterminate & varying delays – not good for transfer of time information!

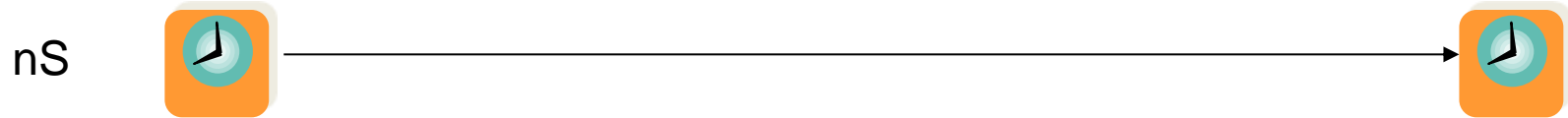
From clocks to packets

- Packet “clocks” are just the same...
- CES Packets do have a regular rhythm – $E1 = 1\text{mS}$
- NTP/PTP Packets may not arrive regularly, but timestamps within the packets themselves mean time information can be extracted
- Time and timing can be distributed from point A to point B



Clock and Time Transfer

- Physical layer, direct connection



- Physical layer, Cascaded PLLs

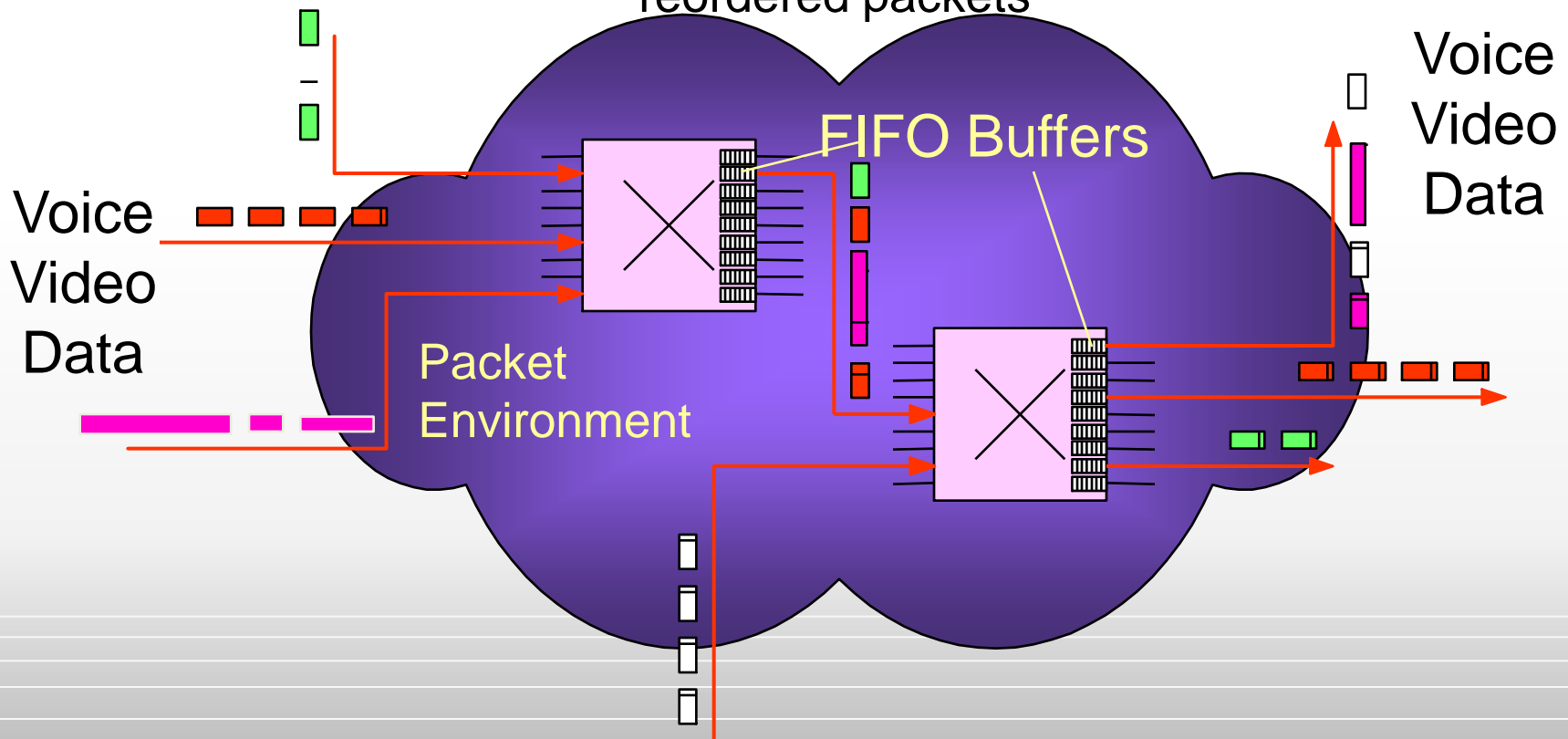


- Packet layer, Cascaded "PLL"s



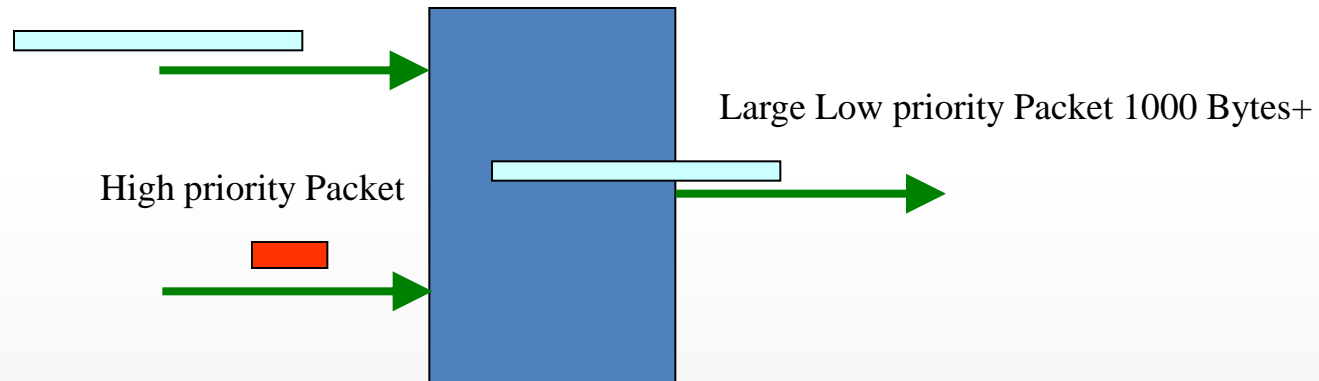
Packet Transport & Switching

Main reason for problems with sync transport across an packet environment is “Packet Delay Variation” and possible lost packets/
reordered packets



Packet Delay Variation

- Even with priority schemes packet delay variation can be significant

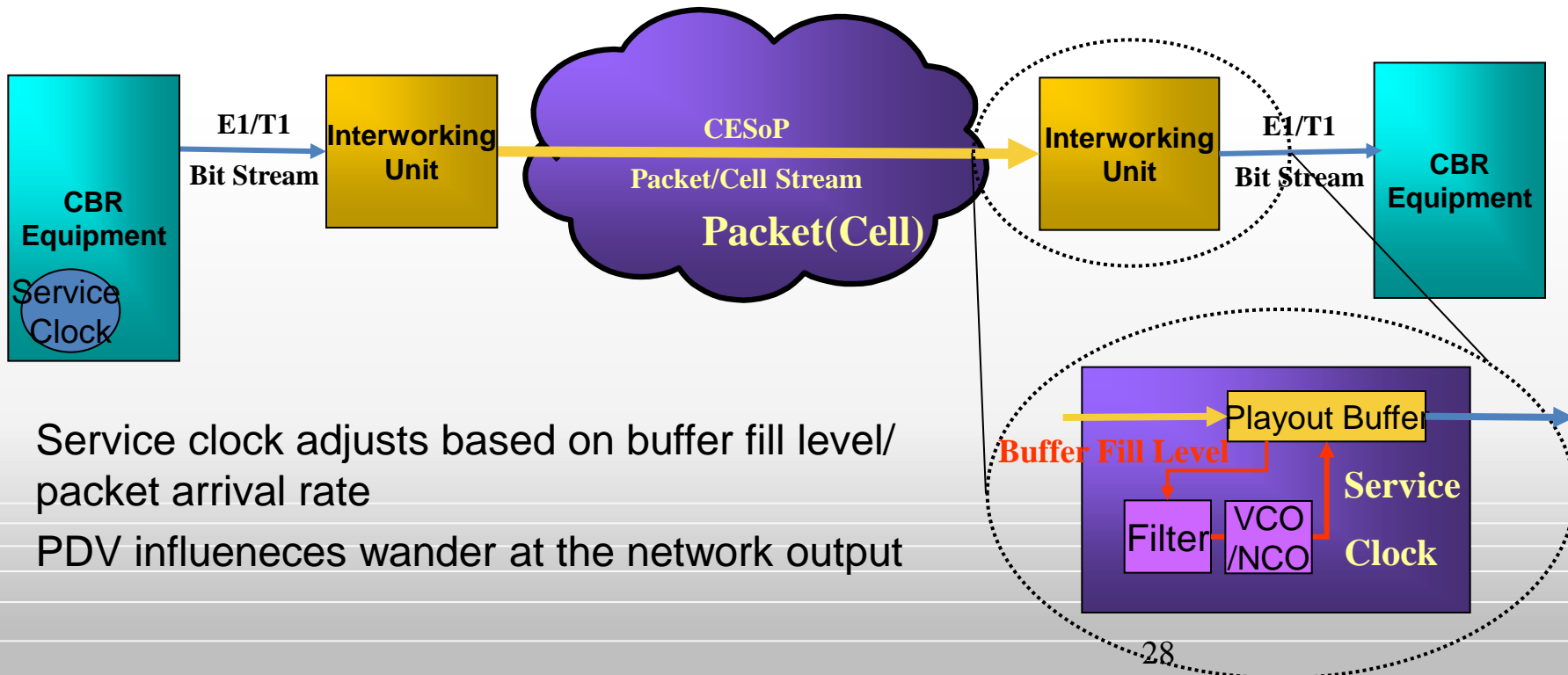


At 100 Mbit/s 1000 byte packet = $8 \times 1000 / 100 \times 10^6 = 80\mu\text{s}$

At 10 Mbit/s 1000 byte packet = $8 \times 1000 / 10 \times 10^6 = 0.8\text{ms}$

Adaptive Clock Operation

- A common network clock may not be available at Packet/(Cell) network boundary
- May not need clock purity provided by network-synchronous and Differential/SRTS methods



- Service clock adjusts based on buffer fill level/ packet arrival rate
- PDV influences wander at the network output

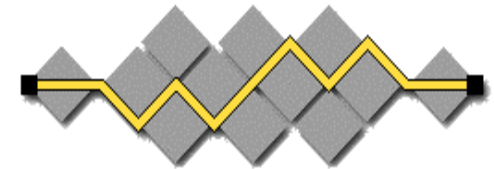
NTP Versions



Features and mechanisms of NTP described in RFCs

“Request For Comments”

the blueprints for the internet

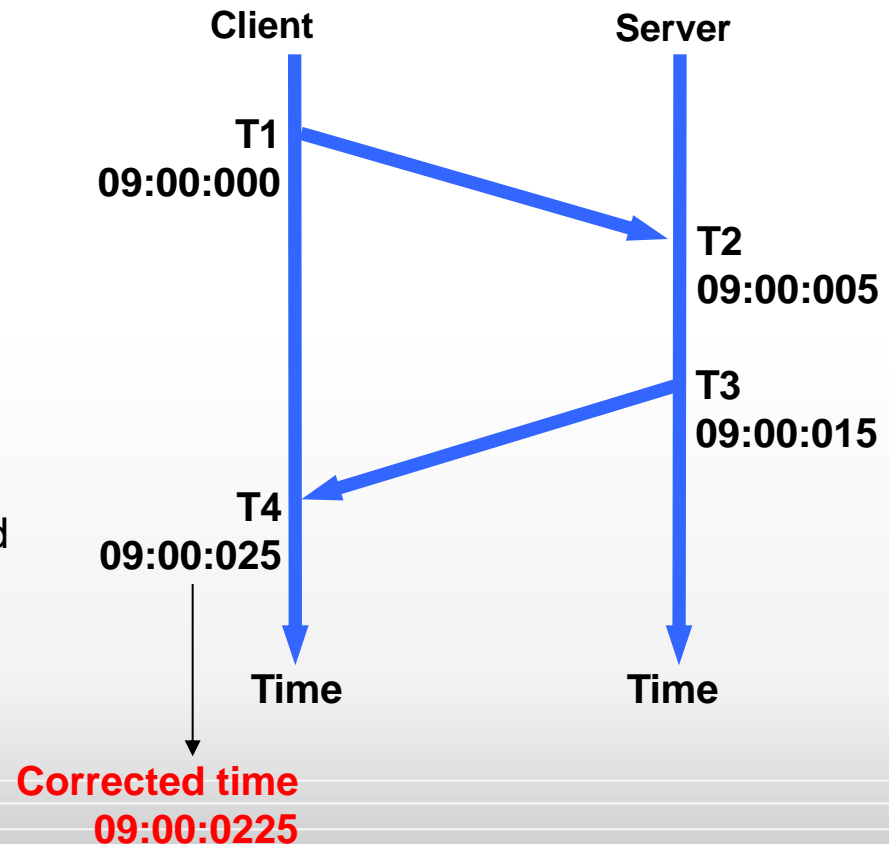


I E T F

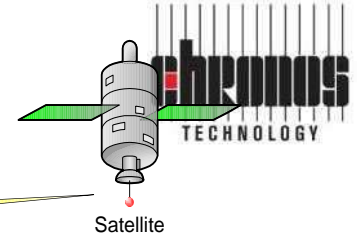
1985	NTPv0	RFC 958
1988	NTPv1	RFC 1059
1989	NTPv2	RFC 1119
1992	NTPv3	RFC 1305
2010	NTPv4	RFC 5905/6/7/8 Security, IPV6, DHCP, MIB
1996	SNTPv4	RFC 2030

How NTP Works

- T1 Originate Timestamp
 - Time request sent by client
- T2 Receive Timestamp
 - Time request received by server
- T3 Transmit Timestamp
 - Time reply sent by server
- T4 Destination Timestamp
 - Time reply received by client
- Round Trip Delay = $(T4 - T1) - (T3 - T2)$
 - Round Trip Delay = $25 - 10 = 15$
- Clock Offset = $[(T2 - T1) - (T4 - T3)] / 2$
 - Clock Offset = $[5 - 10] / 2 = -2.5$
(Client's actual time when reply received was therefore **09:00:0225**)
- **Key Assumptions:**
 - One way delay is half Round Trip (symmetry!)
 - Drift of client and server clocks are small and close to same value
 - Time is traceable (worth distributing!)



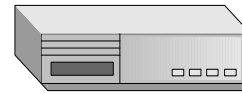
NTP Network Architecture



GPS

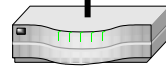


Stratum 1



Time Server

Stratum 2



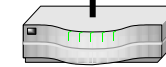
Router



Server



Server



Router

Stratum 3



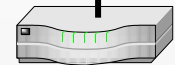
Server



Server



Server



Router



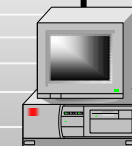
Computer



Computer



Computer



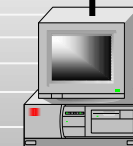
Computer



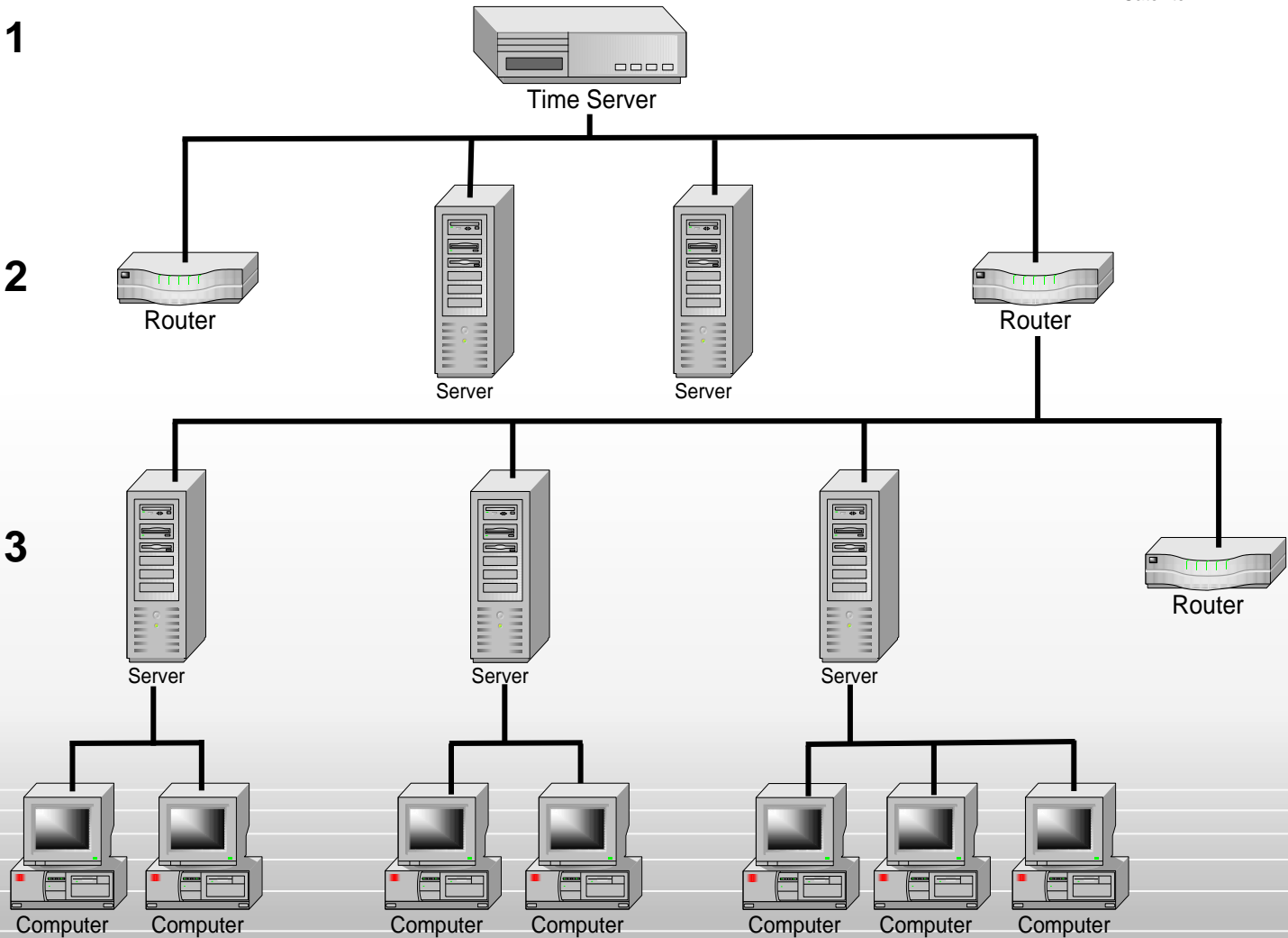
Computer



Computer

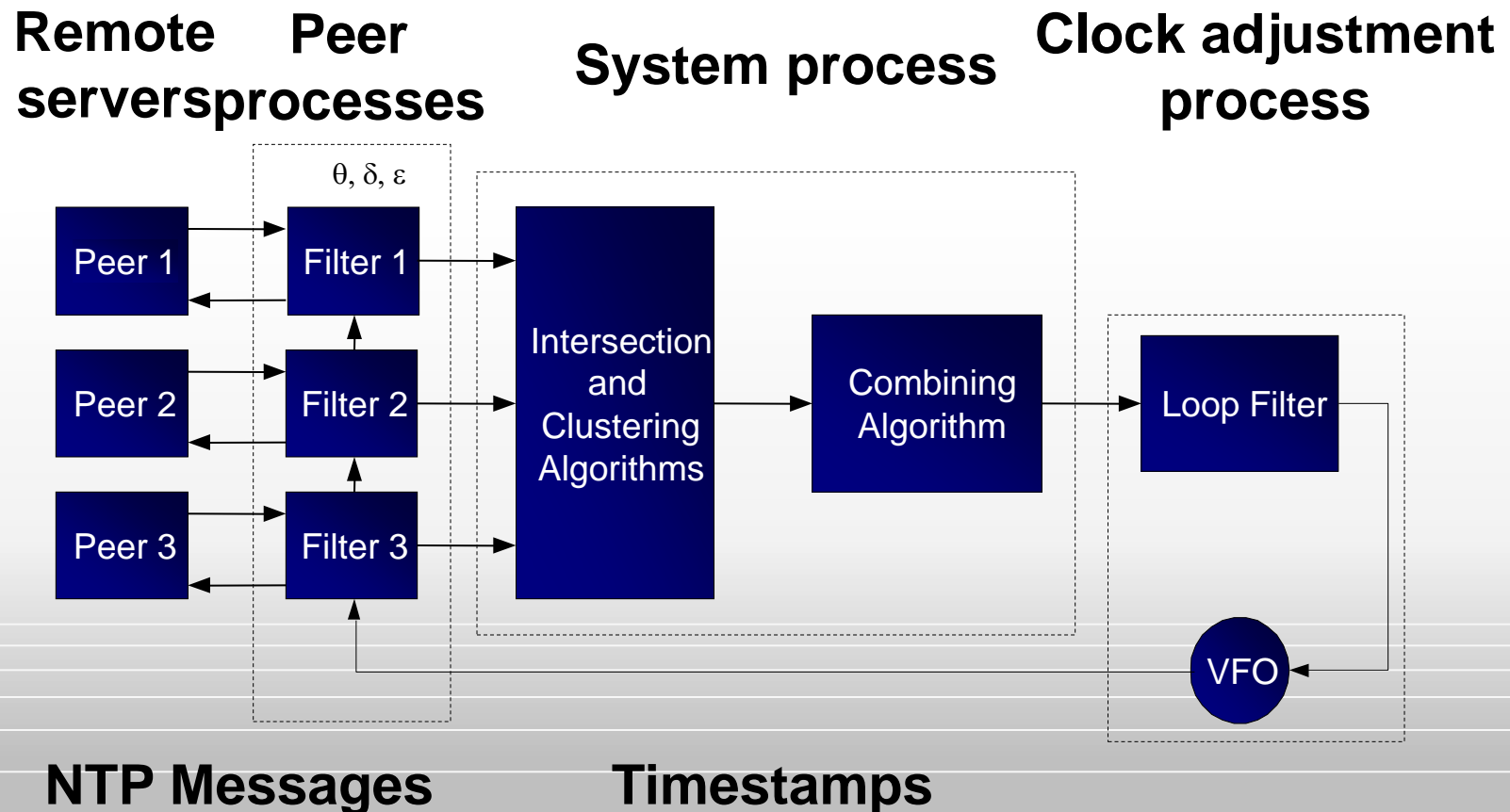


Computer



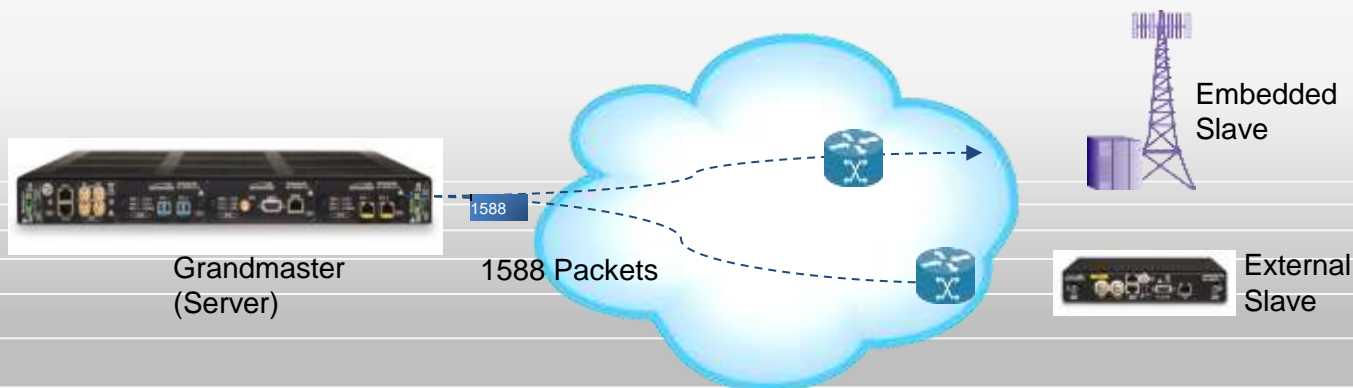
NTP Inputs and Outputs

- Inputs - 3 x sources of equal or higher quality time from peers or servers
- Output - Adjusted time available to peers and clients



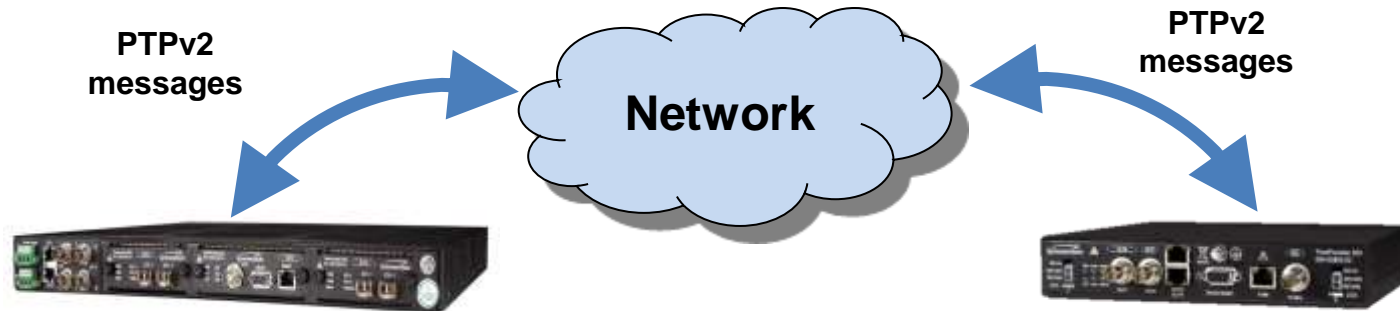
IEEE 1588-2008 PTPv2 Overview

- The Grandmaster “reference clock” sends a series of time-stamped messages to slaves.
- Slaves eliminate the round-trip delay & synchronize to the Grandmaster.
- Frequency is recovered from an accurate time of day reference.
- Accuracy is enhanced by:
 - Frequent packet send rate (up to 128 per second)
 - Hardware time-stamping (eliminate software processing delays)
 - Best Master Clock Algorithm (optional, “best” master voted by nodes)



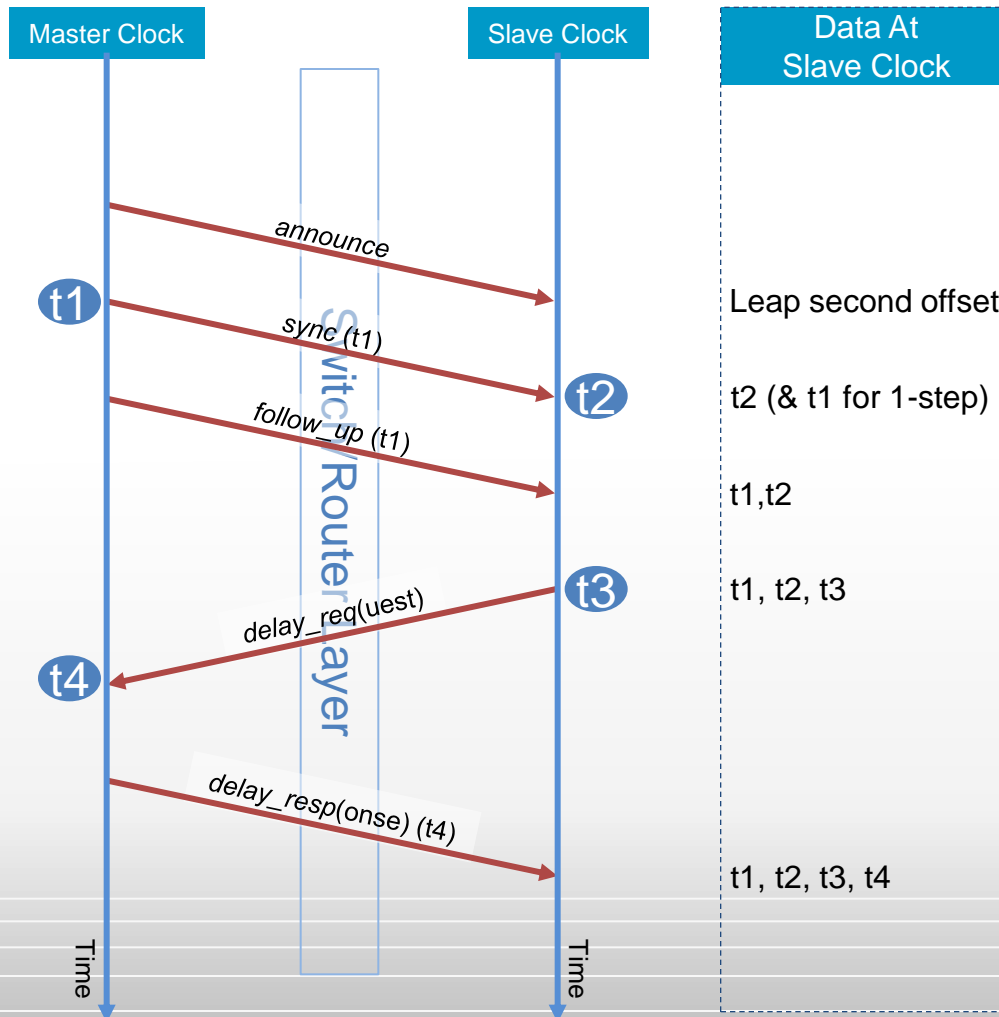
PTPv2 Slave clocks can be either stand-alone or embedded in network equipment

PTPv2 Timing Message Types



- The **Grandmaster** (Server) sends the following messages:
 - Timing Messages (3 types):
 - **Sync** message
 - **Follow_Up** message (optional)
 - **Delay_Resp**(onse)
 - **Announce** message (GM status)
 - **Signaling** (2 types)
 - Acknowledge TLV (ACK)
 - Negative Acknowledge TLV (NACK)
- The **Slave** (Client) sends the following messages:
 - Timing Messages
 - **Delay_Req**(uest)
 - **Signaling** (3 types)
 - Request announce
 - Request sync
 - Request delay_resp(onse)

Time Transfer Technique



Round Trip Delay

$$RTD = (t_2 - t_1) + (t_4 - t_3)$$

Offset:

(slave clock error and one-way path delay)

$$\text{Offset}_{\text{SYNC}} = t_2 - t_1$$

$$\text{Offset}_{\text{DELAY_REQ}} = t_4 - t_3$$

We assume path symmetry, therefore

$$\text{One-Way Path Delay} = RTD \div 2$$

$$\text{Slave Clock Error} = (t_2 - t_1) - (RTD \div 2)$$

Notes:

1. One-way delay cannot be calculated exactly, but there is a bounded error.
2. The protocol transfers TAI (Atomic Time). UTC time is TAI + leap second offset from the *announce* message.

“The Telecom Profile” (G.8265.n/G.8275.n)

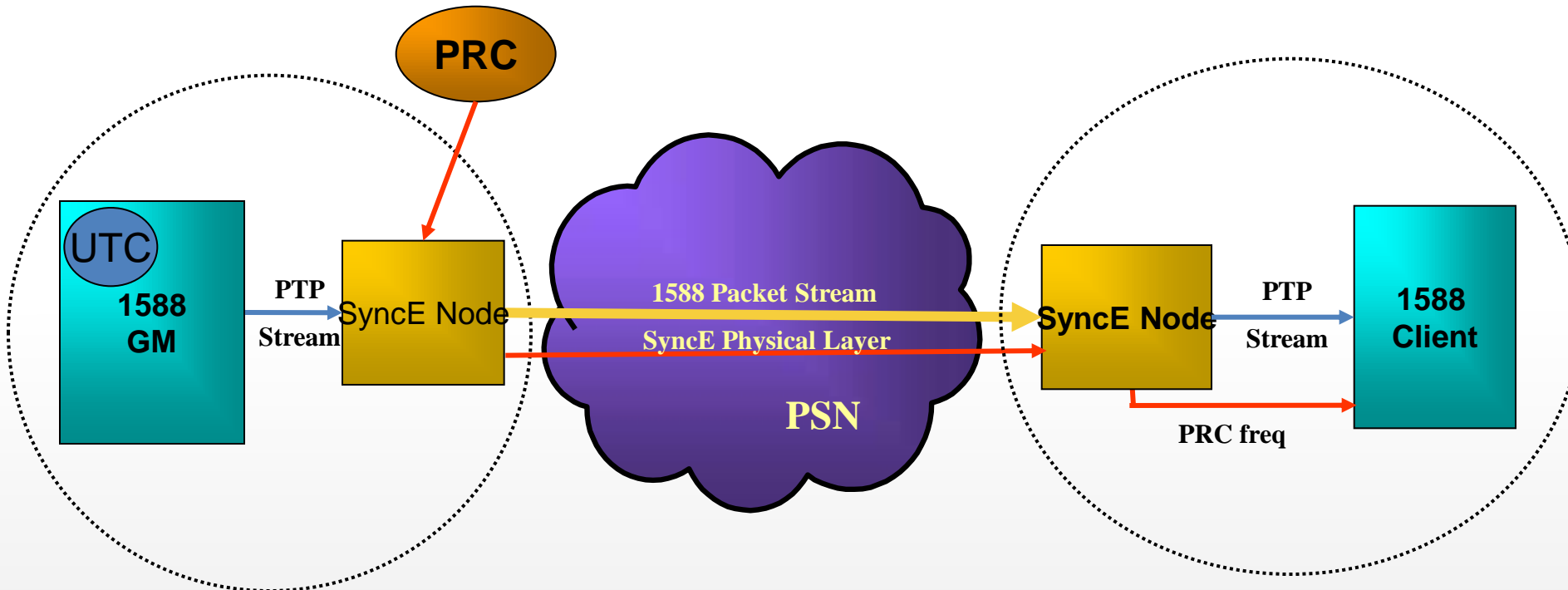
- A profile is a subset of required options, prohibited options, and the ranges and defaults of configurable attributes
 - e.g. for Telecom: Update rate, unicast/multicast, etc.

- PTP profiles are created to allow organizations to specify selections of attribute values and optional features of PTP that, when using the same transport protocol, inter-works and achieve a performance that meets the requirements of a particular application

- *Other (non-Telecom) profiles:*
 - IEEE C37 238 Power Distribution Industry
 - 802.11AS AV bridging (AV over domestic LAN)

Combination Operation

- SyncE as “frequency assistance” to 1588



- Gives immediate “frequency lock” to 1588 client
- SyncE & 1588 functionality may be in the same node/element

Summary

- Physical Layer Sync Distribution
 - Historically frequency, phase
- Packet Layer Sync Distribution
 - Historically time (NTP)
 - PTP (& “carrier class” NTP) add frequency & phase
- Combination operation
 - Using both physical and packet layers to deliver frequency, phase & time with greater accuracy & reliability.

Questions?



Thankyou

www.chronos.co.uk

www.syncwatch.com

Christian.Farrow@chronos.co.uk