Measurements of equipment intended for time synchronization with partial on-path support

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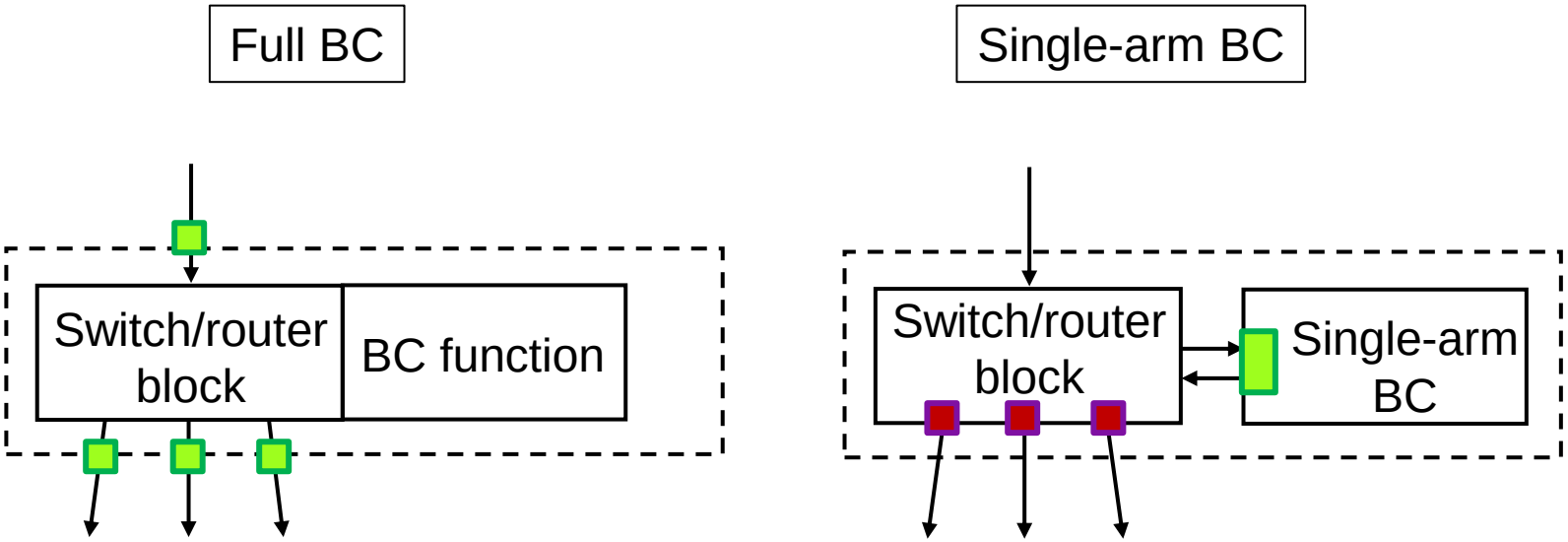
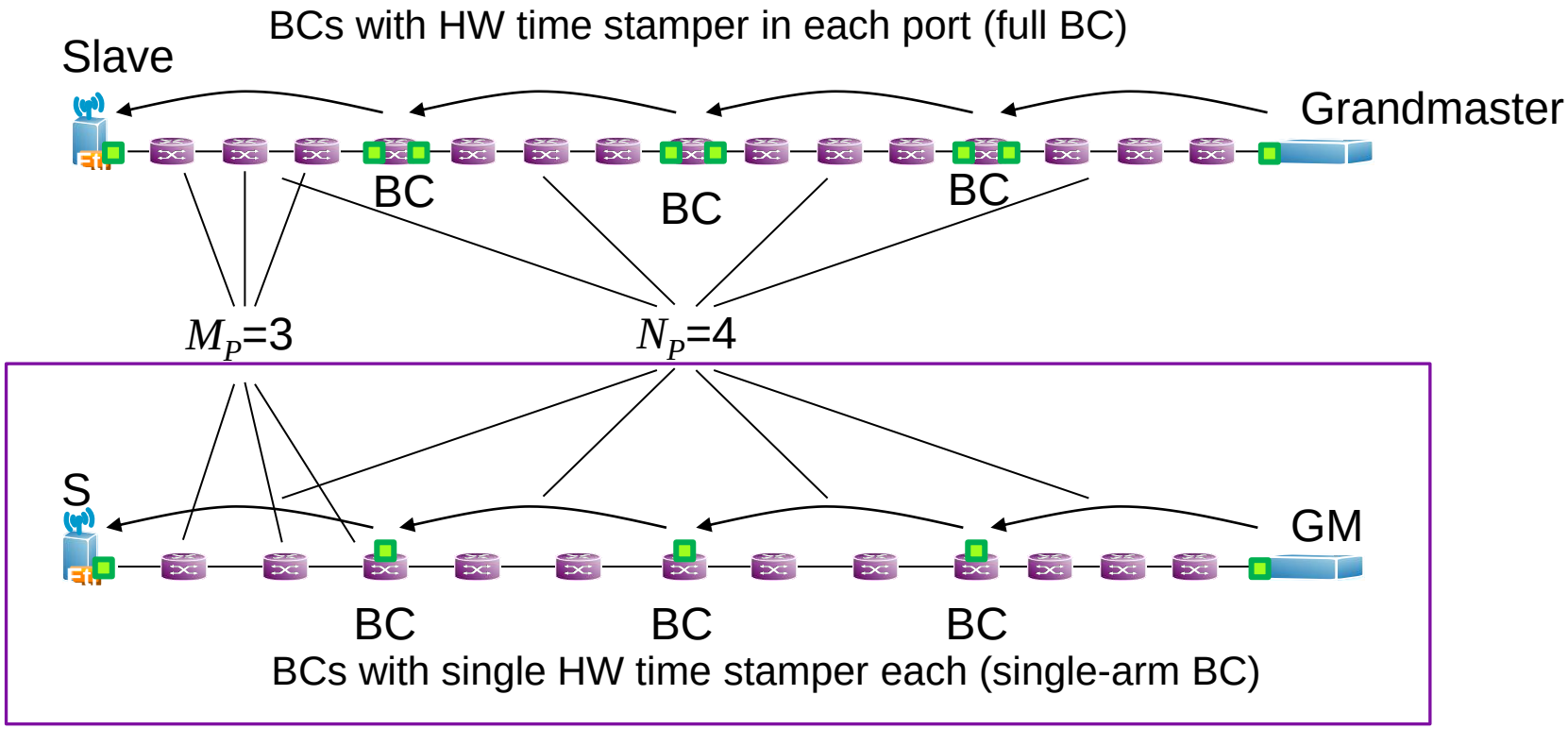
Implementation classes of boundary clocks, BCs

- Although full boundary clock is the ultimate goal, an intermediate solution, single-arm boundary clock is viable.
- All tested equipment were single-arm BCs.

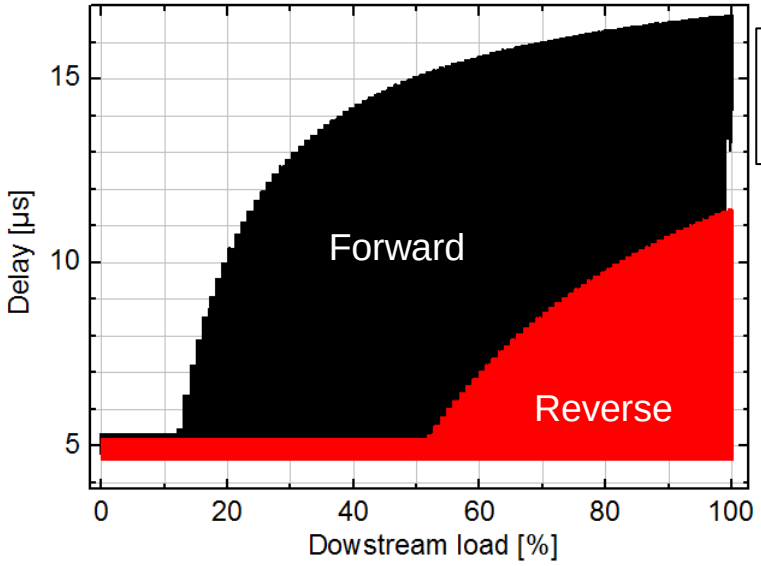


Topology: N_P x M_P = 12 chain

- Earlier studies have indicated that a chain of 12 contended hops with reasonable performance can be achieved if there is a BC after every 3 or 4 contended hops.
- This study concentrates in the case of single-arm BC (lower chain below)

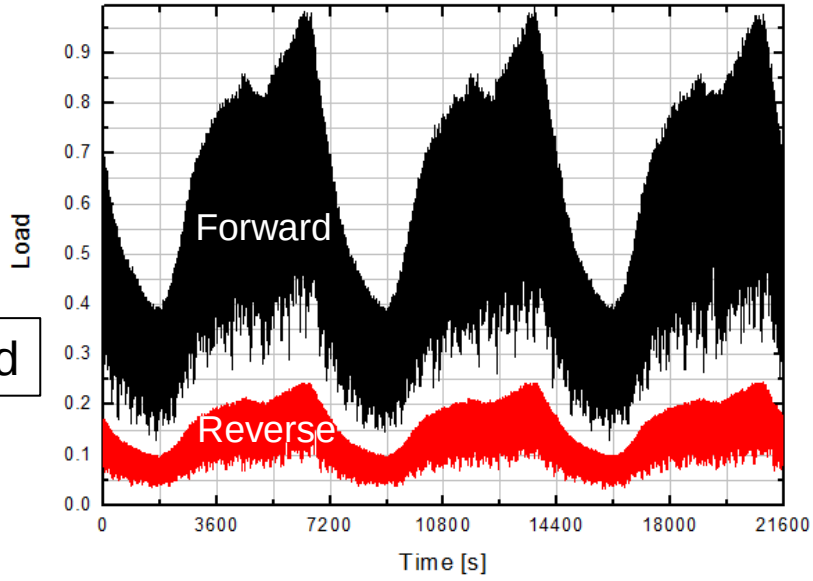


Creating the delay corresponding to three hops

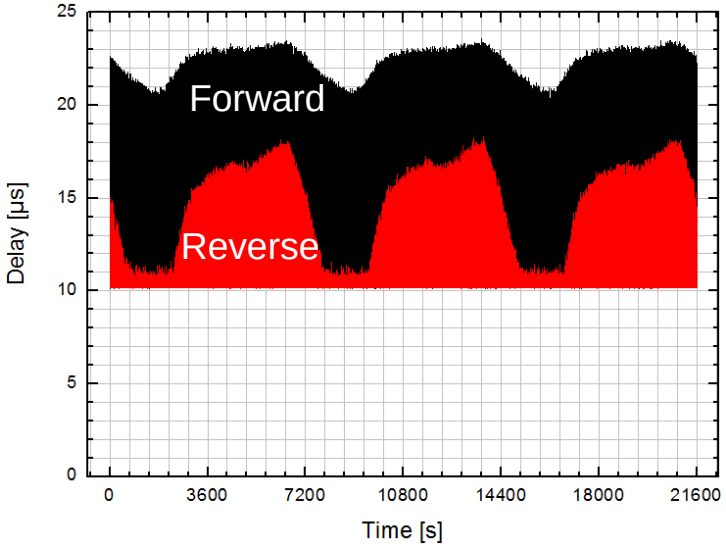


Delay vs. load

Load

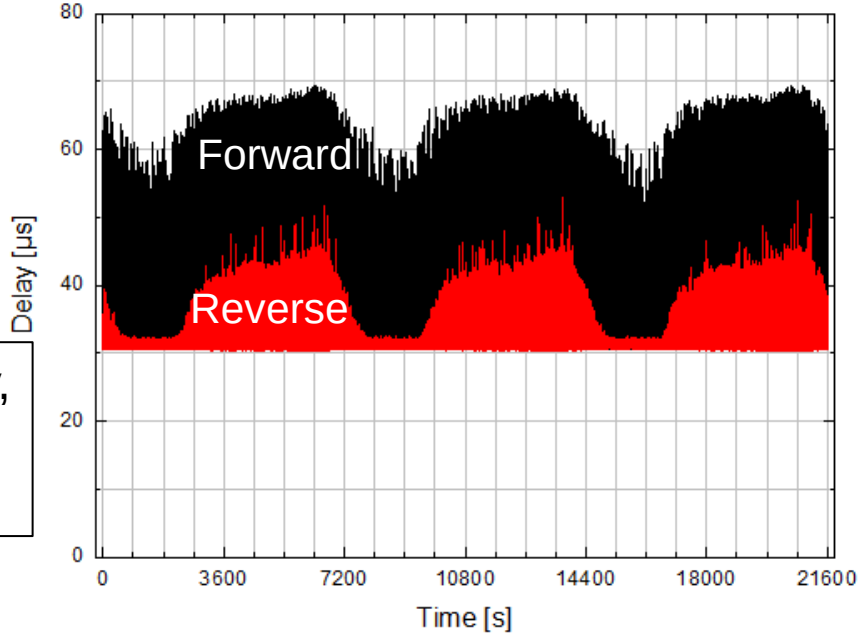


Delay, single hop



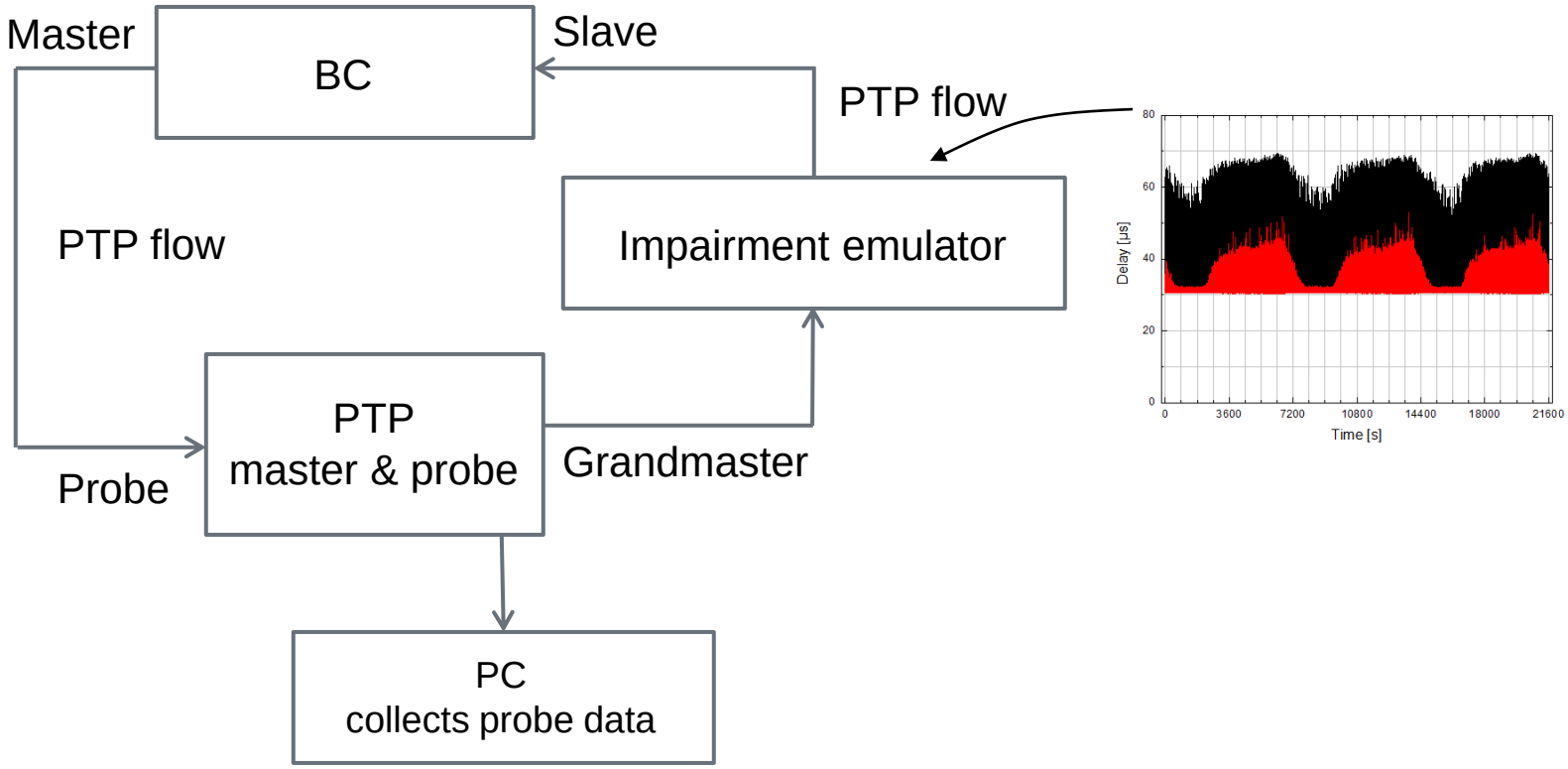
3 x

Delay, three hop



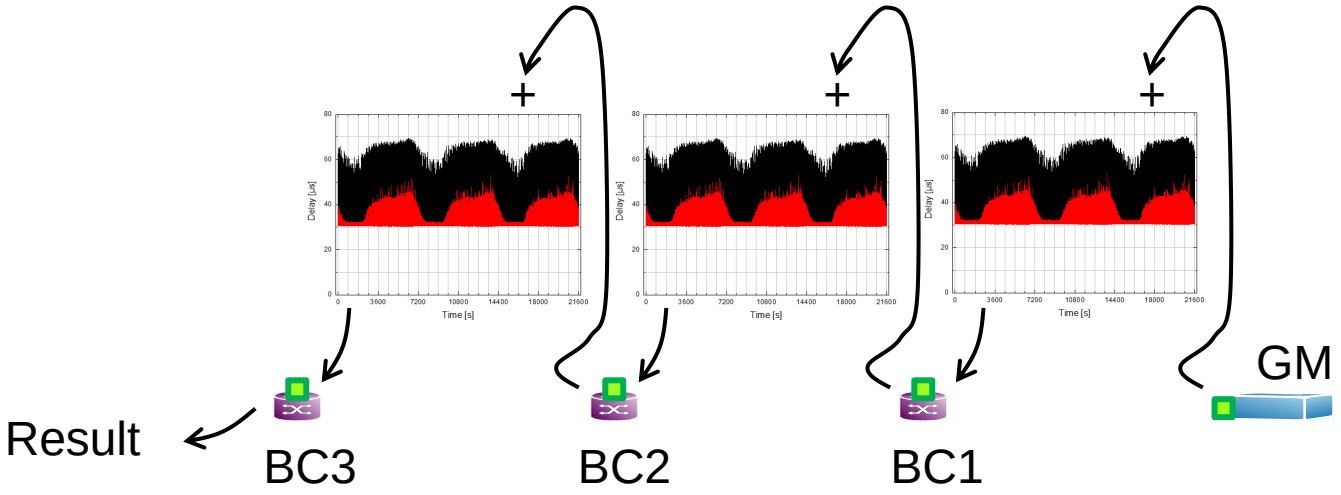
Measurement setup

- The delay forward and reverse delay files were loaded into an impairment emulator.
- The probe measures the apparent forward and reverse delays from the BC master port to the probe. The difference between the fwd and rev apparent delays is dominated by the time error of the BC



Mimicking a chain by multiple measurements of the same BC

- The delay files corresponding to three hops are run in an impairment emulator while the GM and BC1 communicate PTP timing.
- The apparent forward and reverse delays are measured from the output of BC1 and added together with the original delay files to produce a pair of new delay files that are used to impair timing traffic to BC2 and so on.
- Finally the apparent delays of BC3 were measured and analyzed.
- For slave testing the original delay file could be added once more to the apparent delays of BC3 to complete a 12-node chain.



Analysis

- The apparent delays were measured.
- The time error can be calculated from the reverse and forward apparent delays, as follows

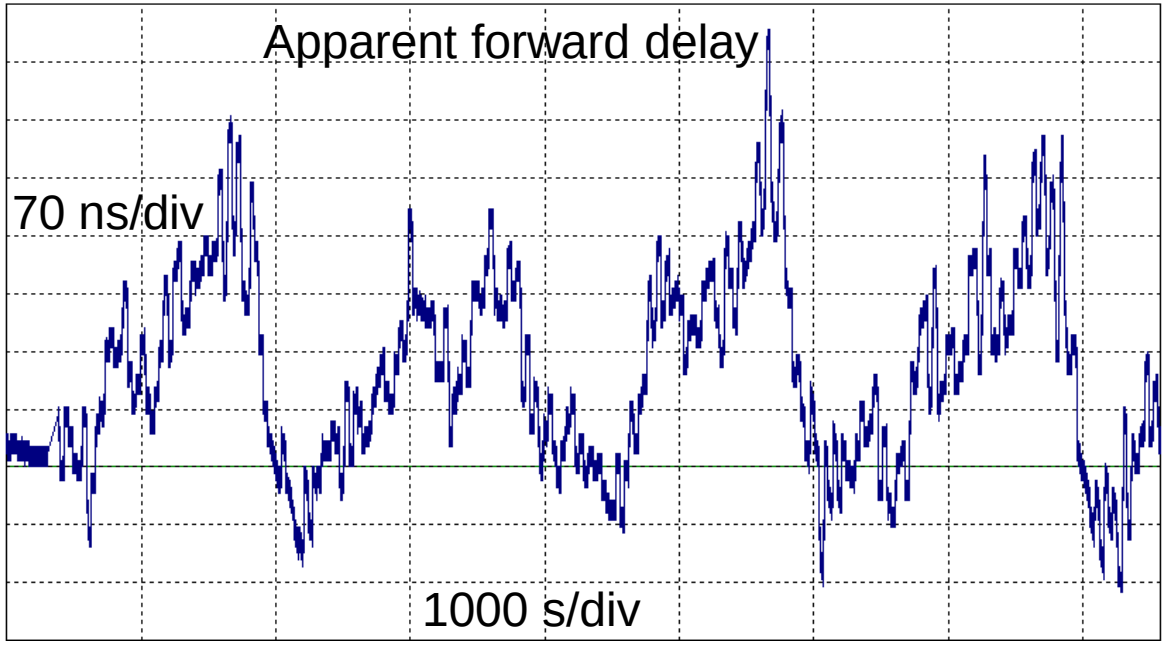
$$\frac{d_{ar} - d_{af}}{2} = Err.$$

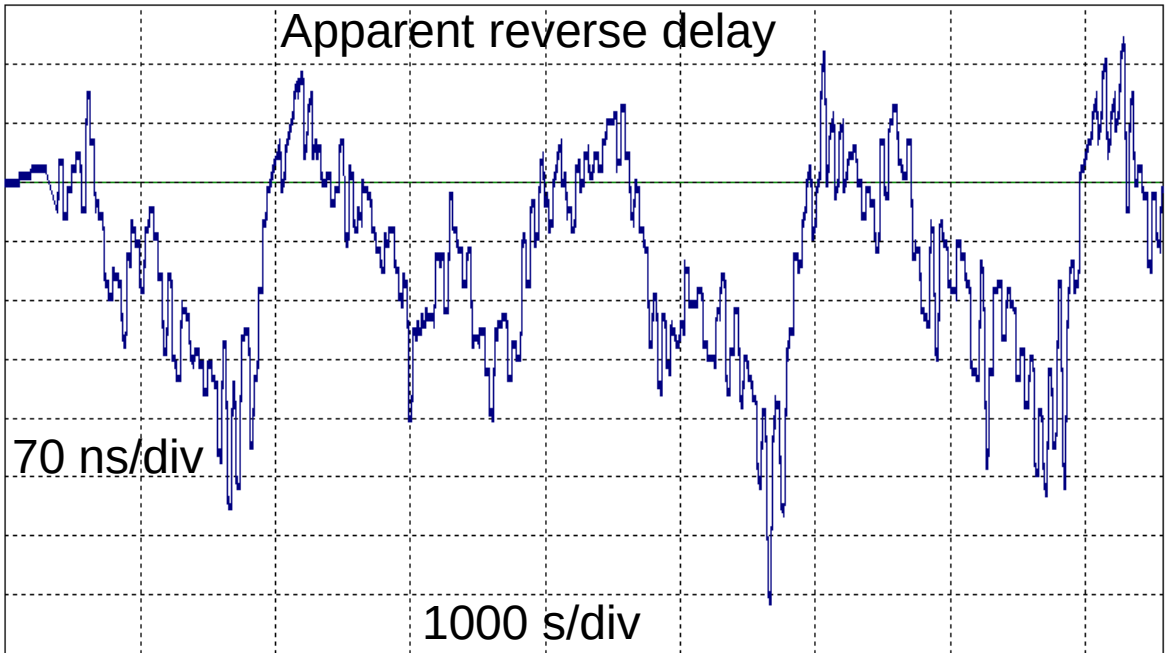
- Since the output of the BCs can be a bit noisy but the floor is steady, the time error analysis was done be selecting the fastest 50 % of packets from 15.625 s windows (1000 packets per window at 64 pps).

BC Vendor A Apparent delays at BC3 output

- Because the time stamps correspond quite accurately to the moment when the Sync is transmitted or Delay_Rec received, the following holds approximately

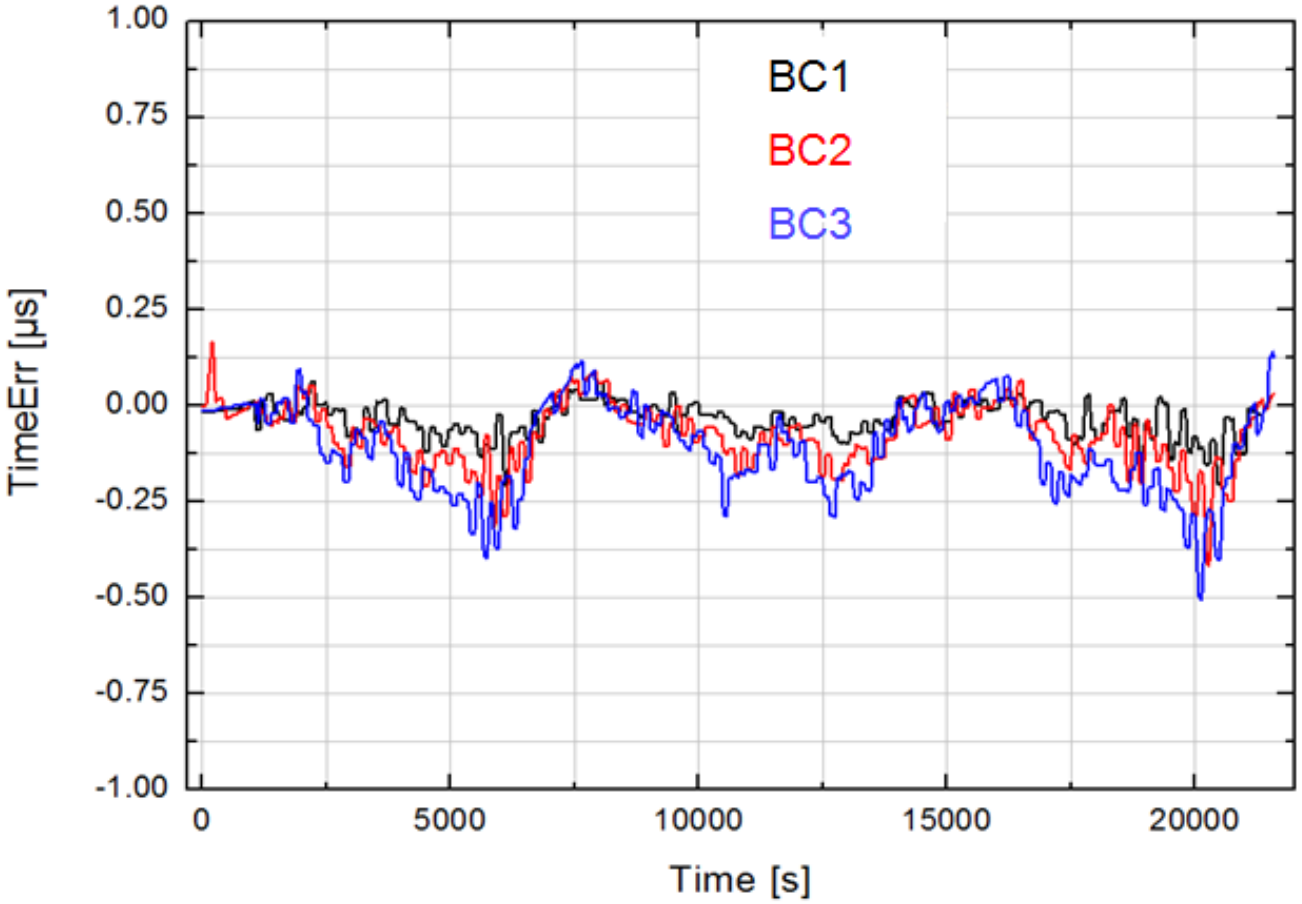
$$d_{ar} = -d_{af} = Err.$$





BC vendor A: Accumulation of time error

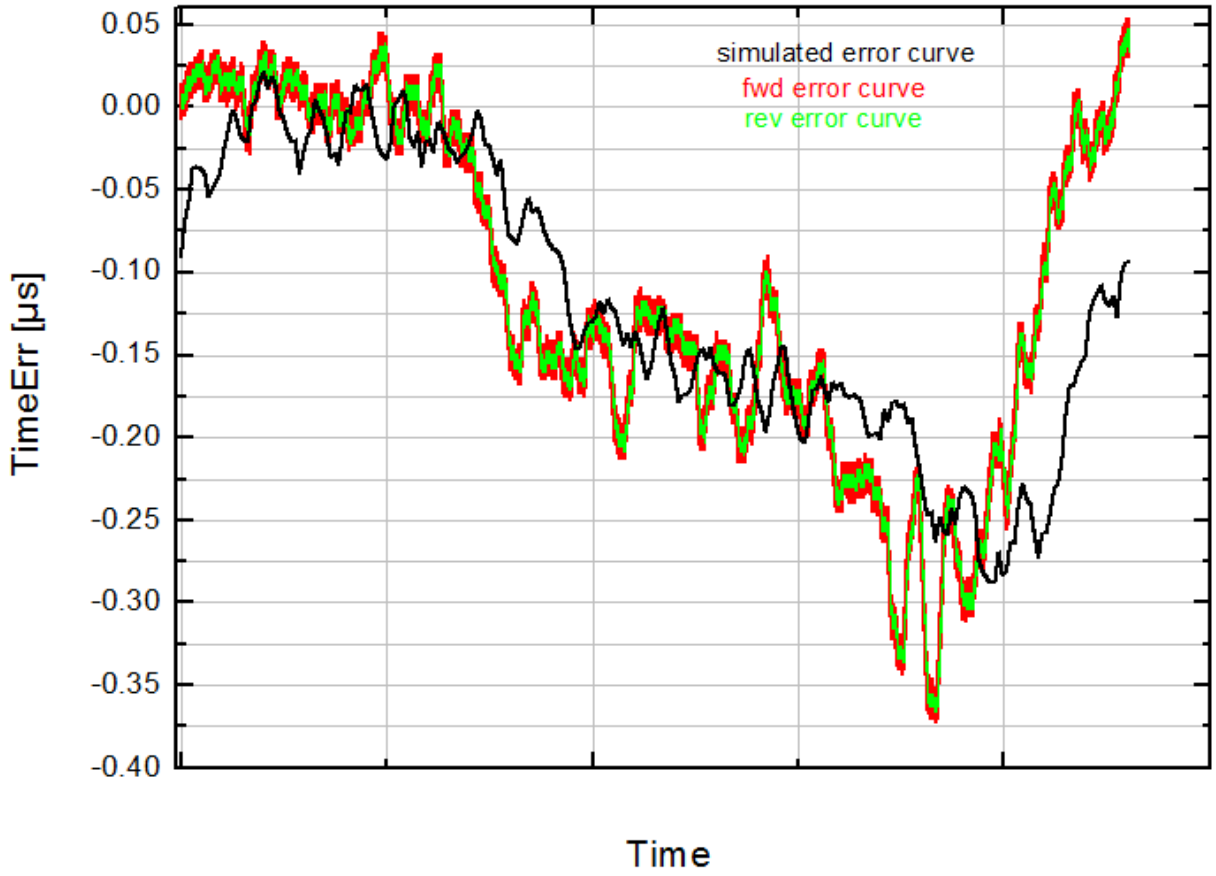
- The noise in the error is relatively large compared with the total amplitude.
- There is clearly time error also with positive sign although the delay files should produce only negligible positive time error.



BC vendor A comparison of performance vs. expected

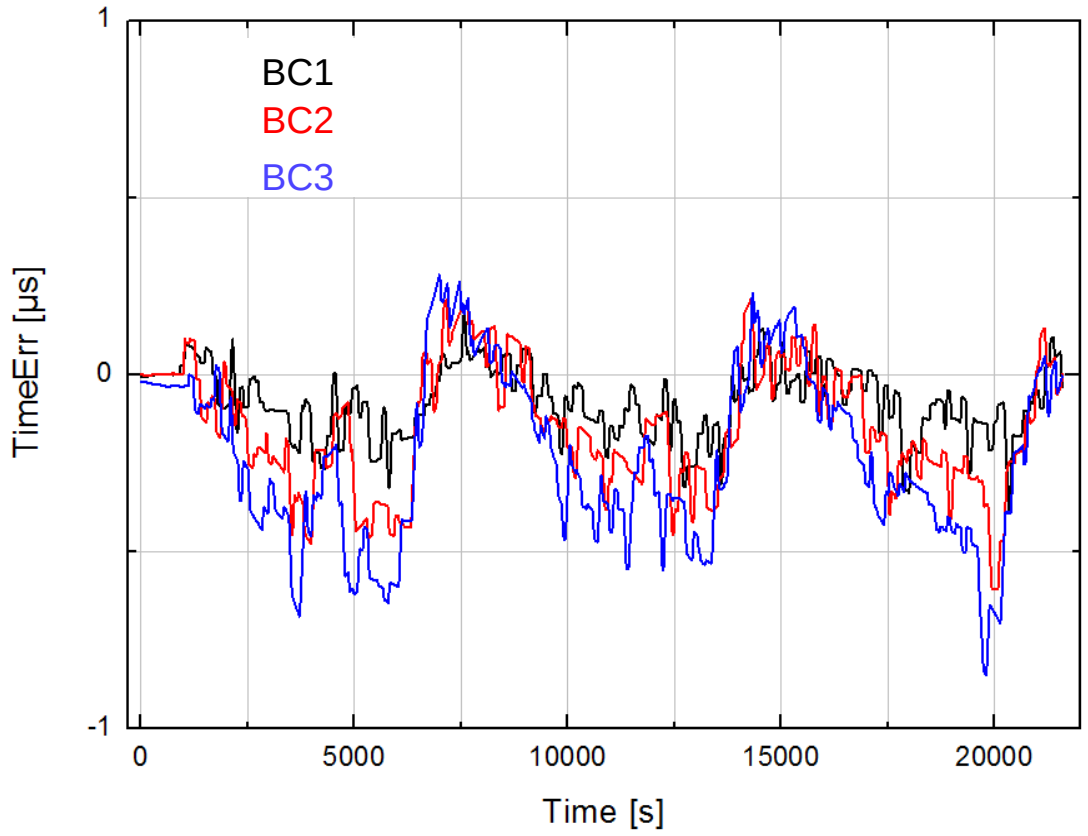
Comparison of measured time error with time error estimated by simulating the BCs with a filtering function: 0.3-% packet selection from 30-s windows and further 120-s averaging.

- The simulated curve (black) coincides with the measured (colored) performance.



BC vendor A: Accumulation of time error (PDV x 2.5)

- Since the error was not approaching error budgeted to PDV effects, the PDV challenge was increased.
- The time error increases by less than half, which hints toward some nonlinearity in the algorithm.

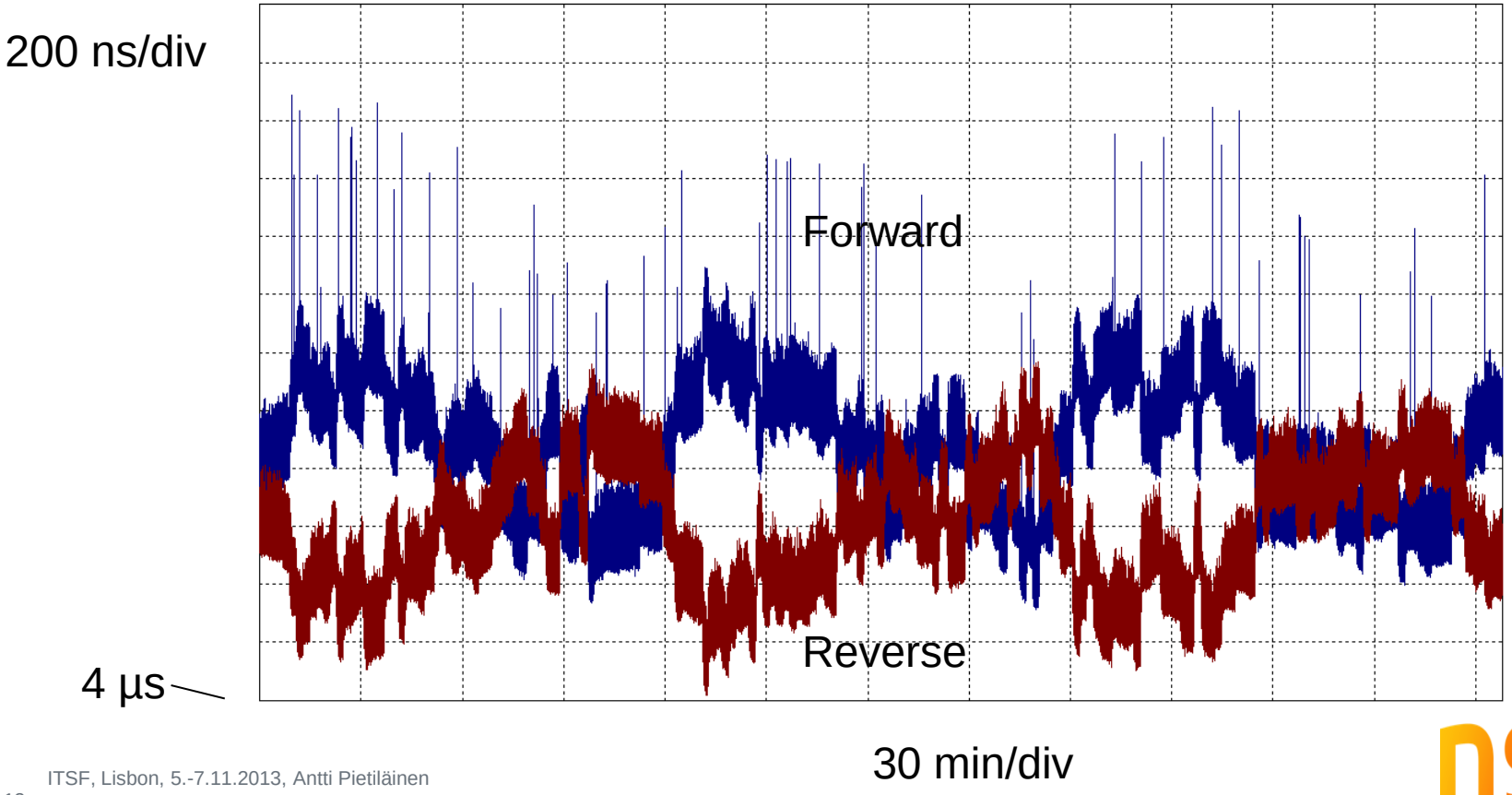


BC vendor B – apparent delays at BC3 output (PDV x 2.5)

- Both forward and reverse apparent delays have ~4.8 µs offset. Thus

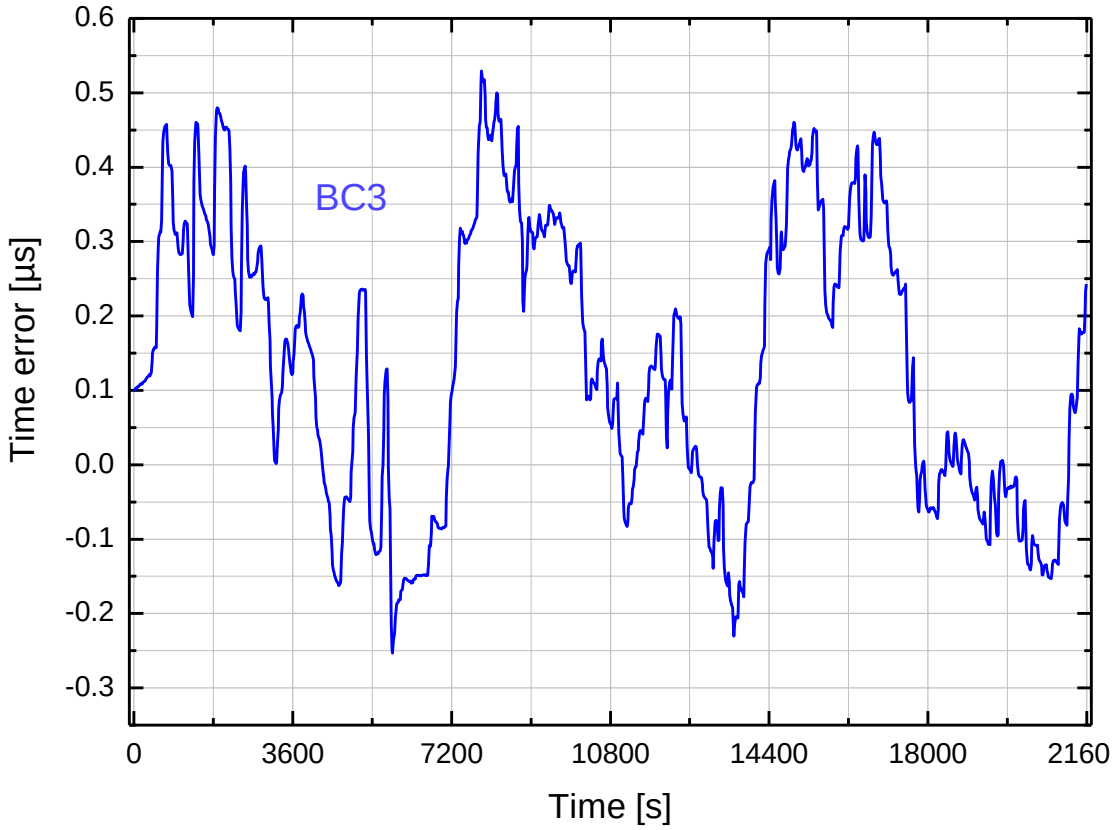
$$d_{ar} \neq -d_{af} \neq Err.$$

- However, the equation $\frac{d_{ar} - d_{af}}{2} = Err$ still holds and the common offset does not affect time accuracy.



BC vendor B - Time error (PDV x 2.5)

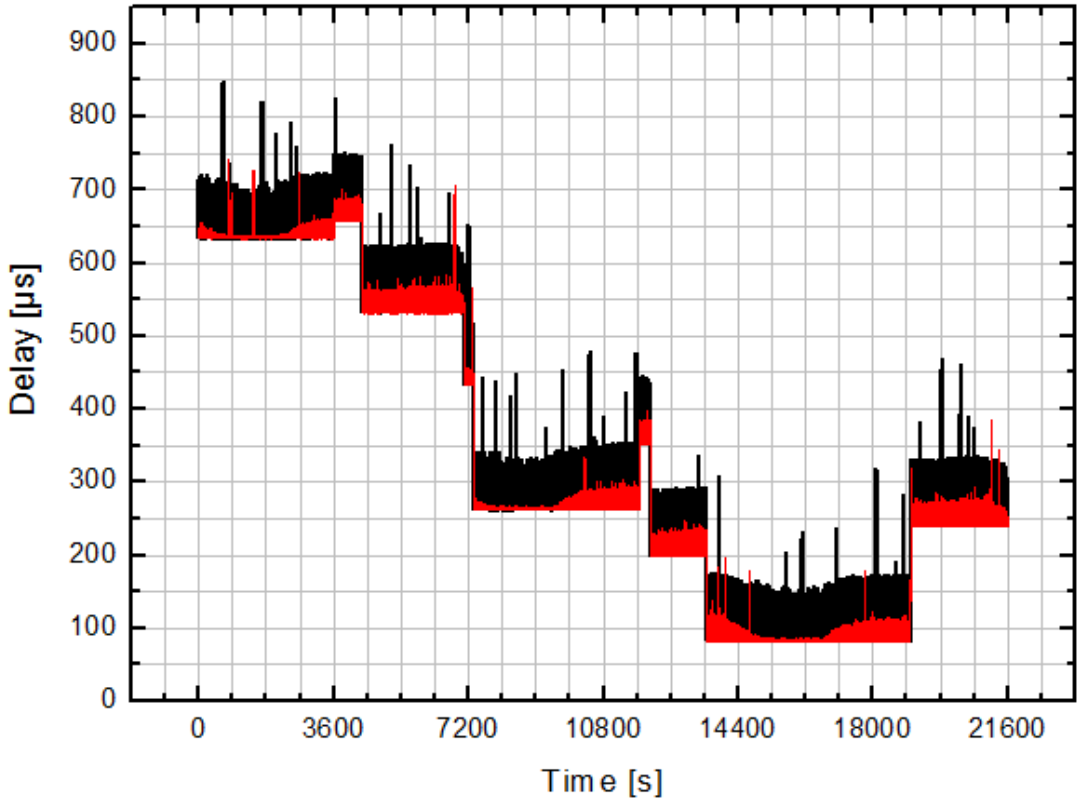
- The error remains small. However, there is clear positive offset though it was expected that the positive error would be small.



Increasing the challenge

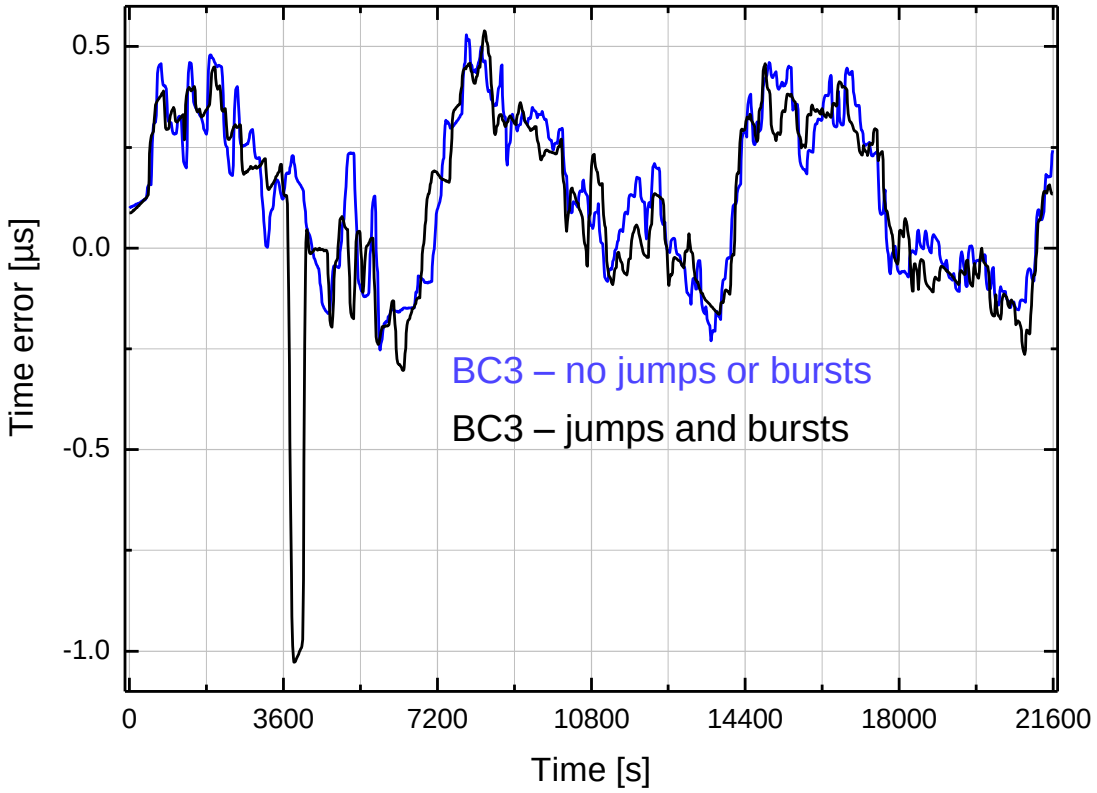
Symmetric delay jumps and asymmetric bursts up to 15 s in length were added to the file that is used to test BC3.

- 9 delay jumps, 44 forward bursts, and 19 reverse bursts
- BC vendor 2 and 3 were tested with the same file pair. Vendor 1 was not tested.



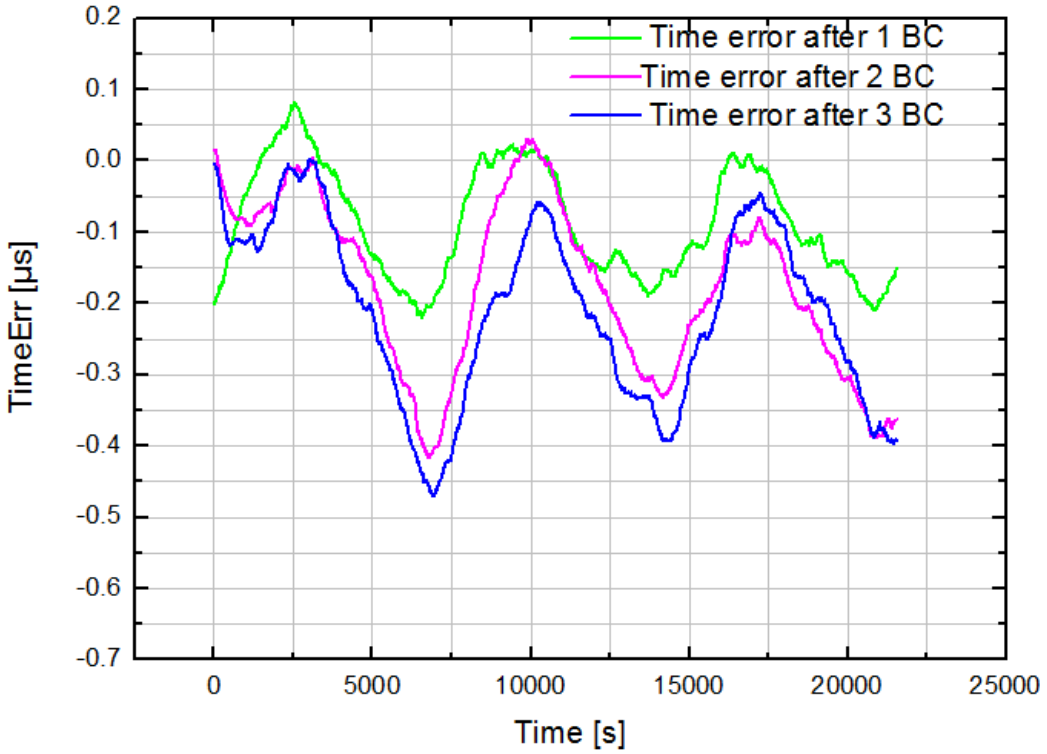
BC vendor B – With jumps and bursts (PDV x 2.5)

- The first delay jump causes a time error extrusion. However no other extrusions were observed even though the experiment was run in a loop almost 3 x 21600 s and thus the same delay jump was repeated two more times.
- The bursts did not affect the time error.



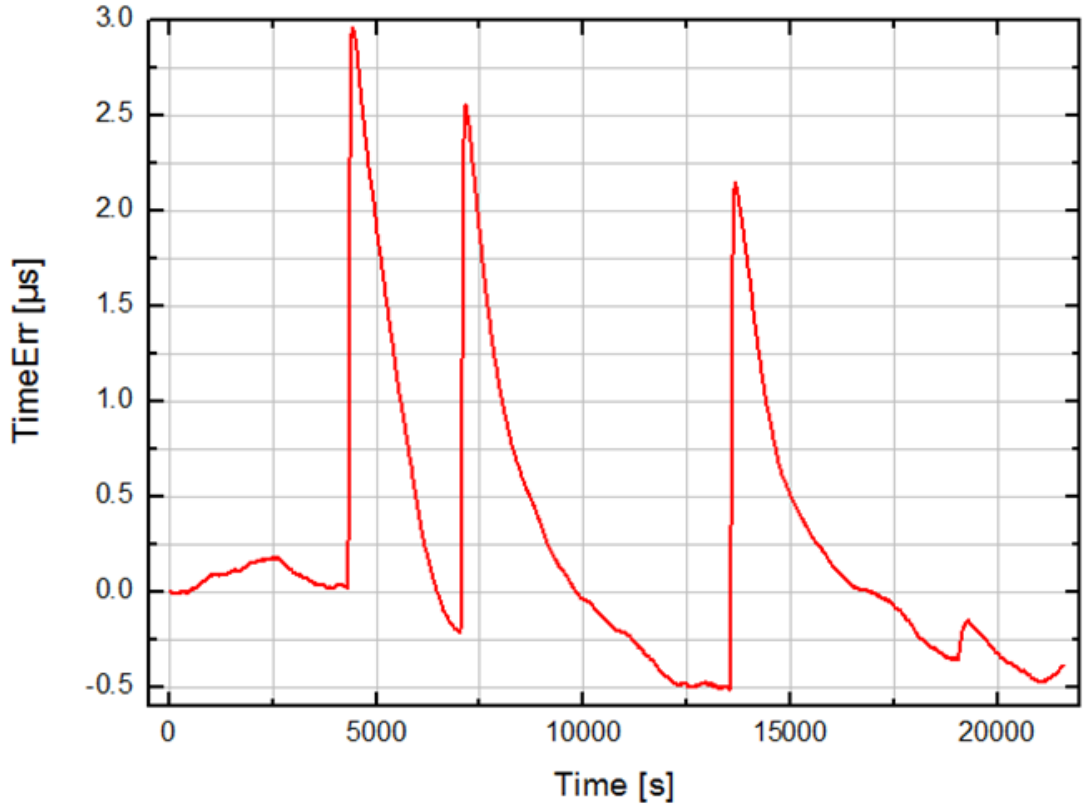
BC vendor C – No jumps or bursts (PDV x 2.5)

- The time error is approximately the same as in case of vendors A and B, though the noise in the error is smaller, maybe due to lower PLL bandwidth.



BC vendor C - With jumps and bursts (PDV x 2.5)

- Three of the delay jumps caused time error extrusions.
- When the 21600-s delay file was run a second time in a loop the extrusions occurred with the same jumps but with different amplitudes.



Conclusions – testing partial on-path support BCs

- Three boundary clocks from three different vendors were tested.
- All BCs operated well when jumps were not added. They did not create excess time error except for a bounded noise component.
- The absence of any peculiar effects (encountered in frequency synchronization tests) was a pleasant surprise.
- When a very challenging delay jump & burst sequence was added:
  - Some of the symmetric jumps caused time error extrusions but most were encountered with no effects to time error.
  - None of the asymmetric delay bursts had an effect to the time error.
- To conclude, the algorithms seem to be quite mature.
- Final note, semi-fixed delay asymmetries and temperature effects that consume the error budget too, were not investigated in this study.