# VERIFICATION OF LAST INCH ARCHITECTURES FOR CORRECT-BY-CONSTRUCTION TIMING

Calnex

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# Acknowledgements

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- Aviral Shrivastava, Arizona State University
- Hugo Andrade, National Instruments
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- Ya Shian Baboud, NIST Gaithersburg
- Marc Weiss, NIST Time and Frequency
- Kevin Stanton, Intel Corporation

# Overview

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- “Correct-by-construction” temporal semantics
- Reminder of an existence proof
- What will it take?
- Testbed proposal
- Conclusions

# What is meant by timing that is "correct-by-construction"?

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Designers of embedded systems, especially distributed embedded systems, should be able to design, simulate, and code generate for multiple targets with guaranteed timing!

# How is timing achieved today?

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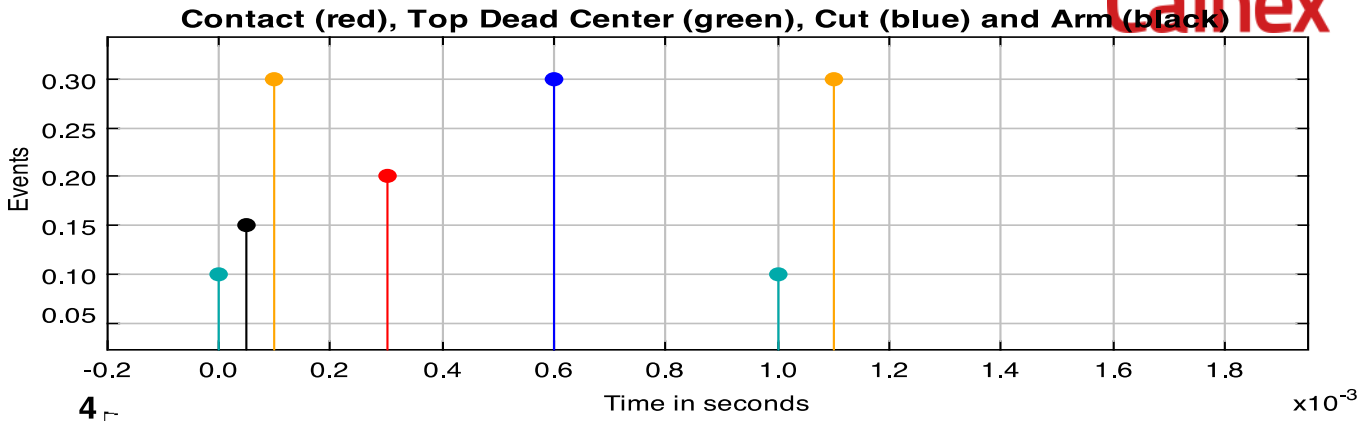
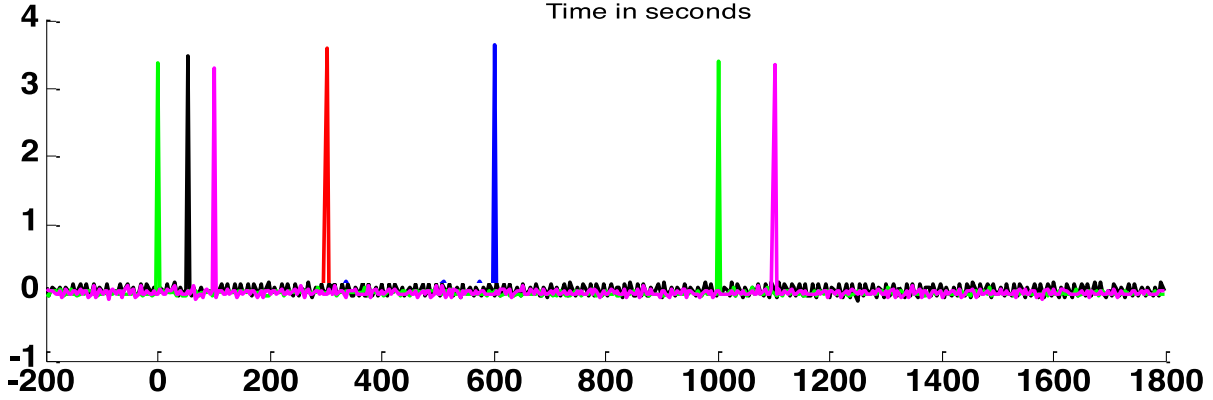
- One current method is carefully constructed bounded-WCET code plus extensive testing followed by frozen design and implementation
- All timing in hardware e.g. FPGA
- Potential “correct-by-construction” techniques:
  - Time triggered architectures e.g. PROFINET
  - PTIDES-like architectures (see next two slides)

# EXISTENCE PROOF: Renesas vs. XMOS: I/O timing (from ISPCS 2013 report on work at UC Berkeley)

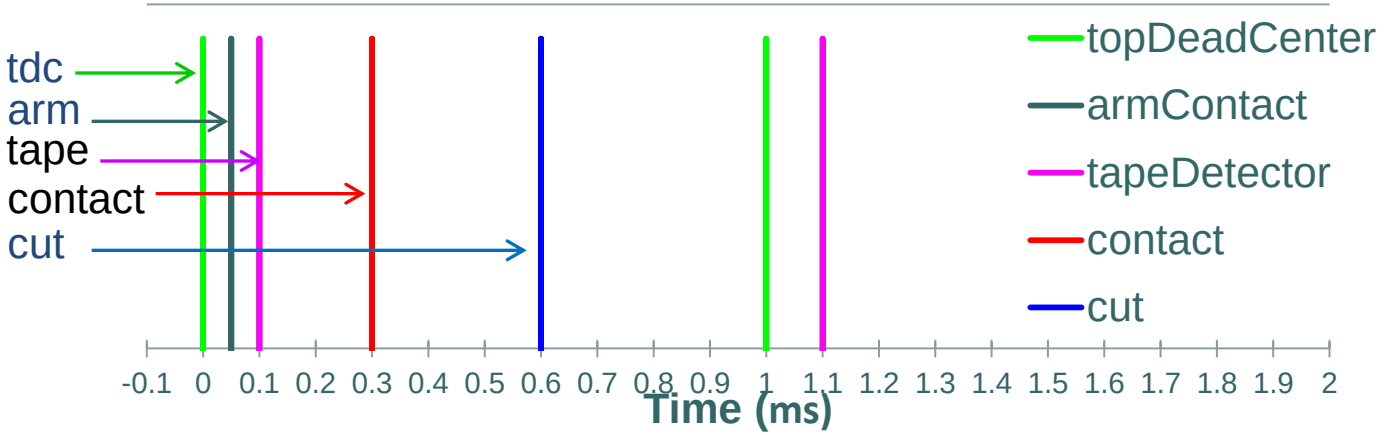
Simulation




Renesas

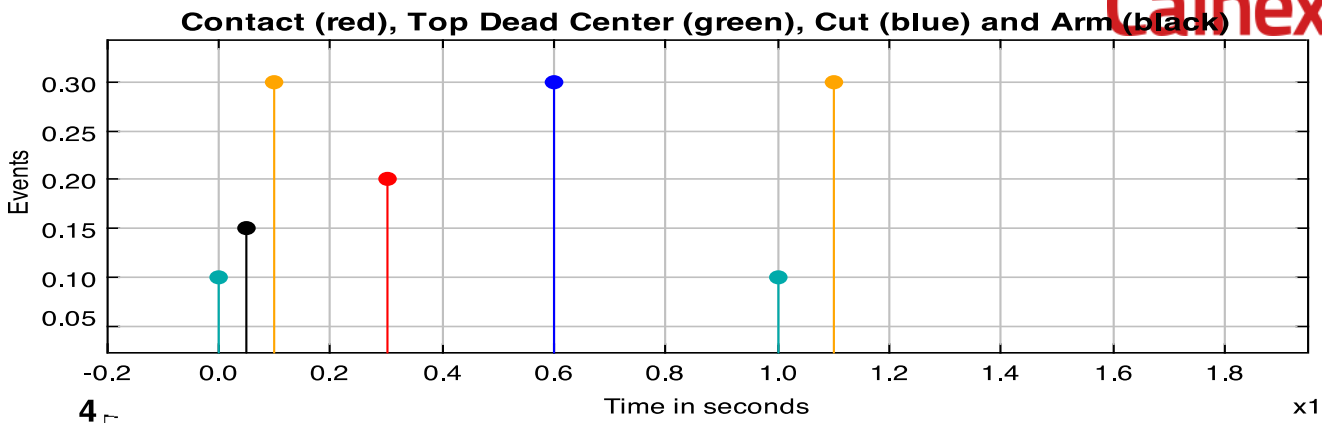



XMOS

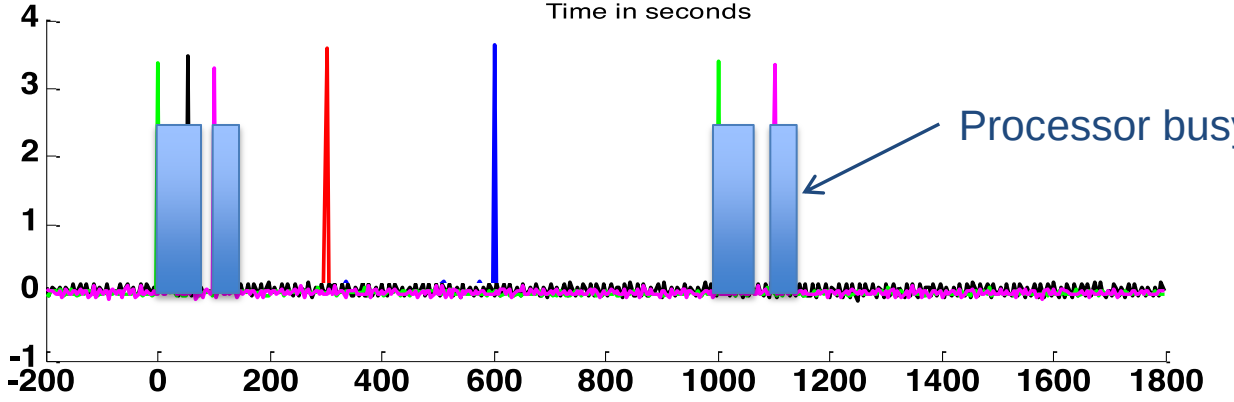


# Renesas vs. XMOS: Busy vs. Idle Time

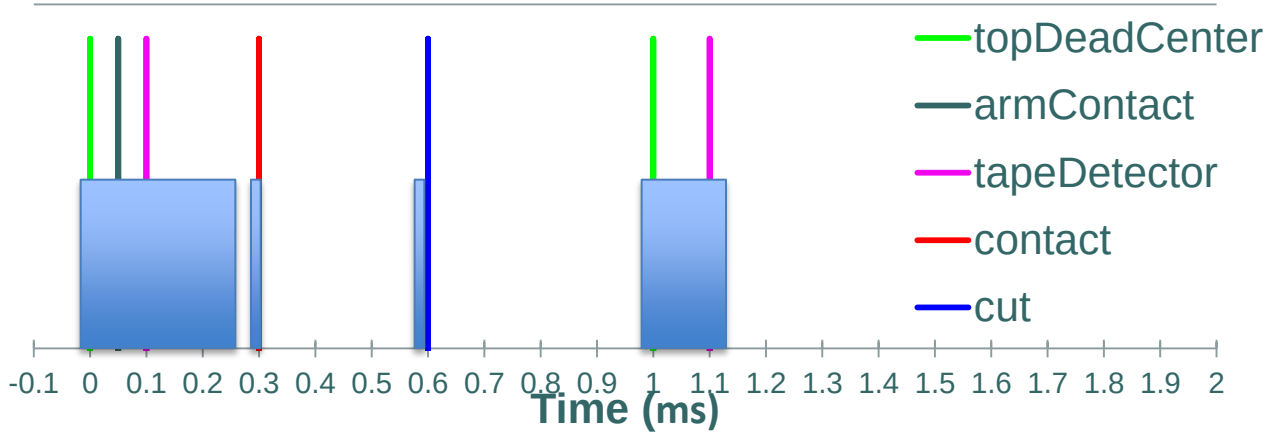
Simulation




Renesas




XMOS
(single core
execution)



# “Correct-by-construction” restrictions

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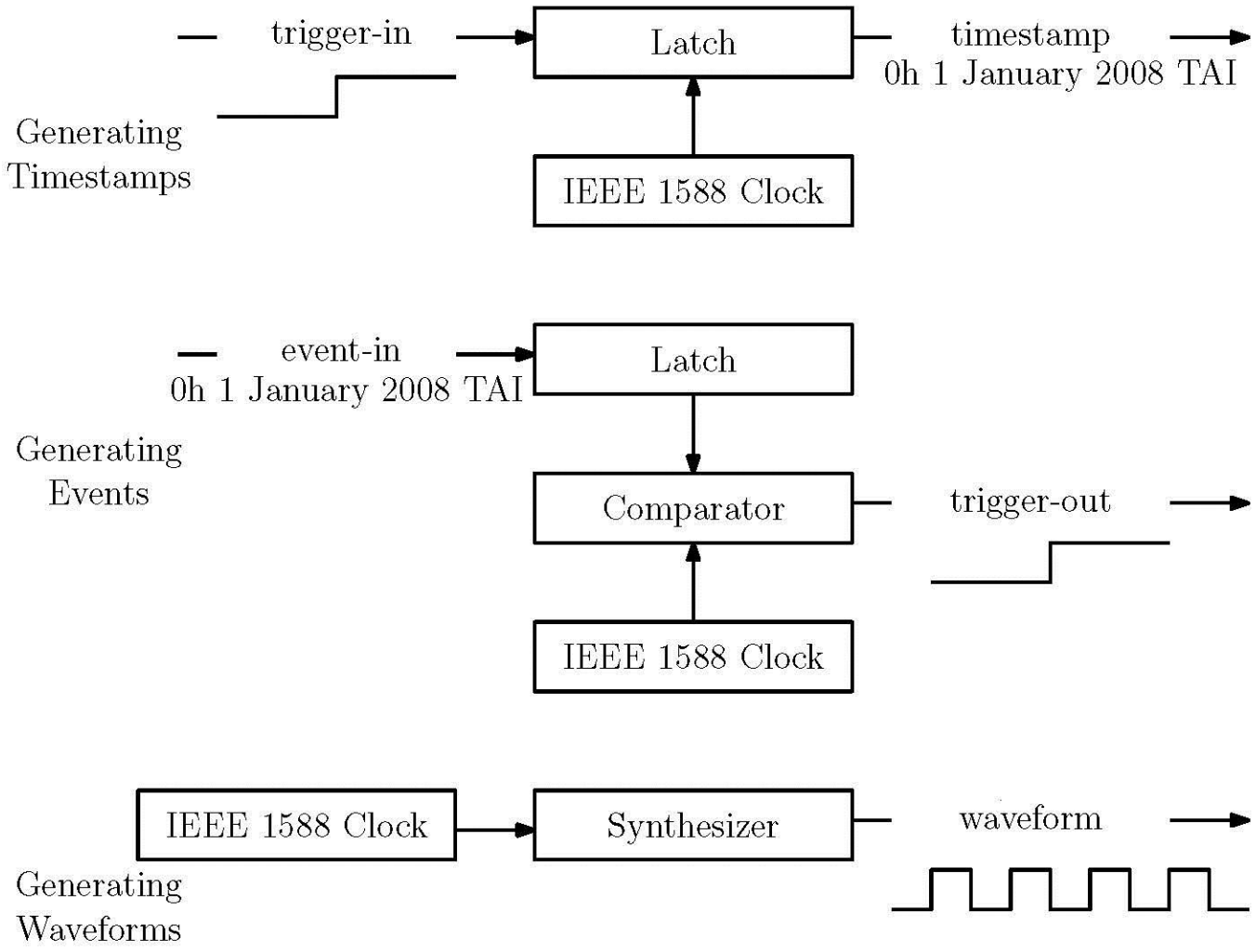
- Requires bounded temporal density of I/O and network traffic (closed world)
- Requires bounded WCET and network latency
- Timing enforcement is done in hardware timing primitives.
- Code timing is not strict except for bounded WCET.

# Timing Primitives



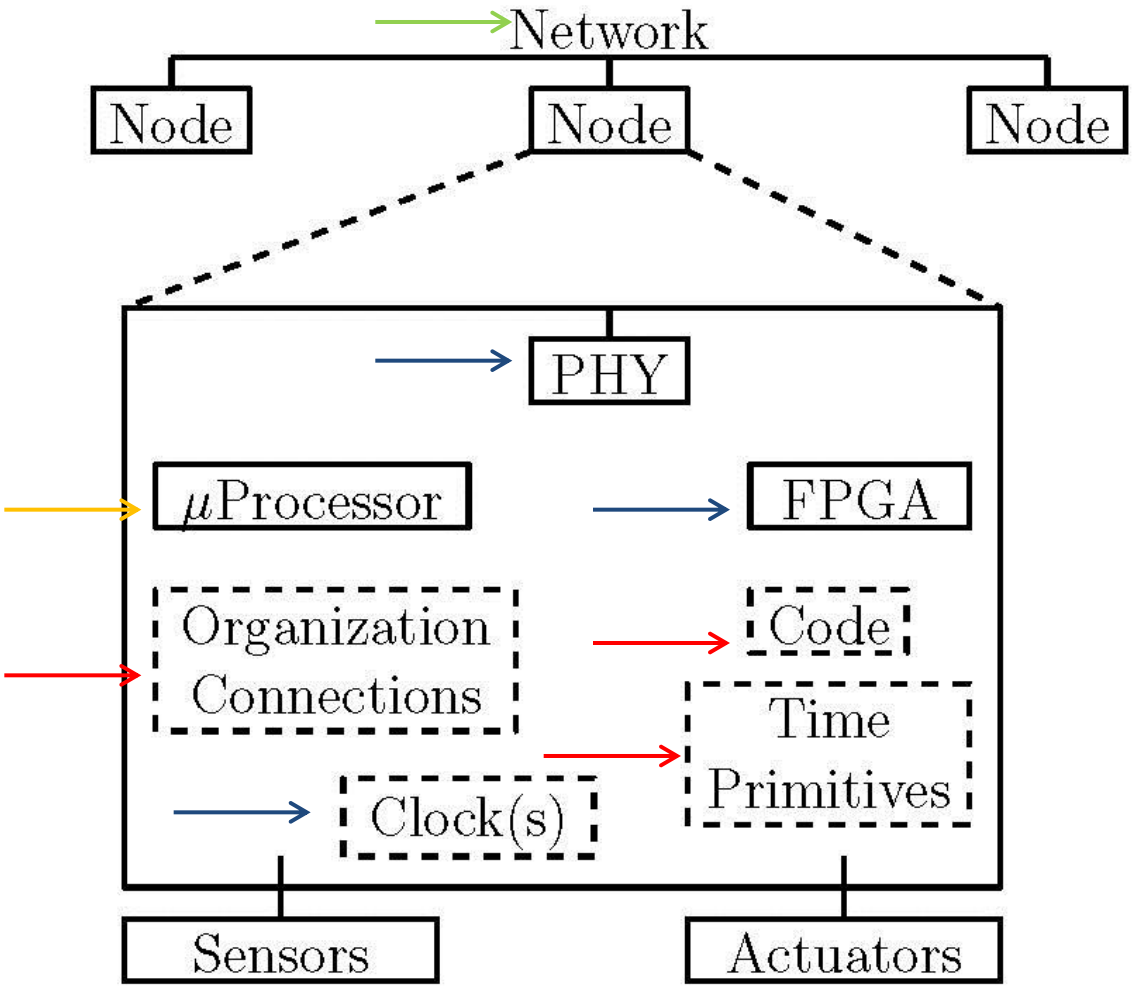
# To achieve a correct-by-construction design environment, we must sort out this mess!

~OK →

Improving →

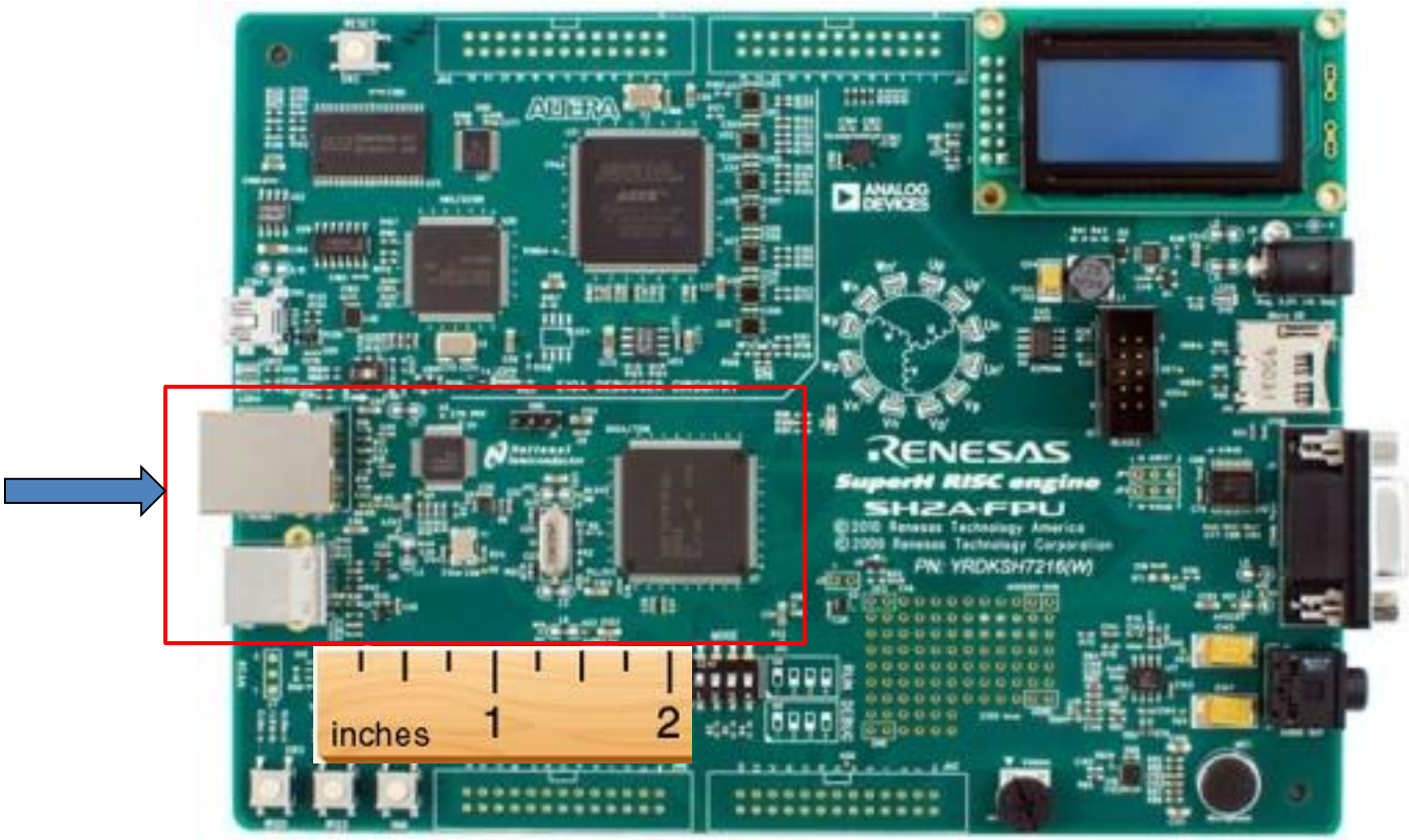
Glimmer of hope →

Lots to be done →



# And on a real board this stuff looks like this

This is the stuff of the previous slide



# The Testbed

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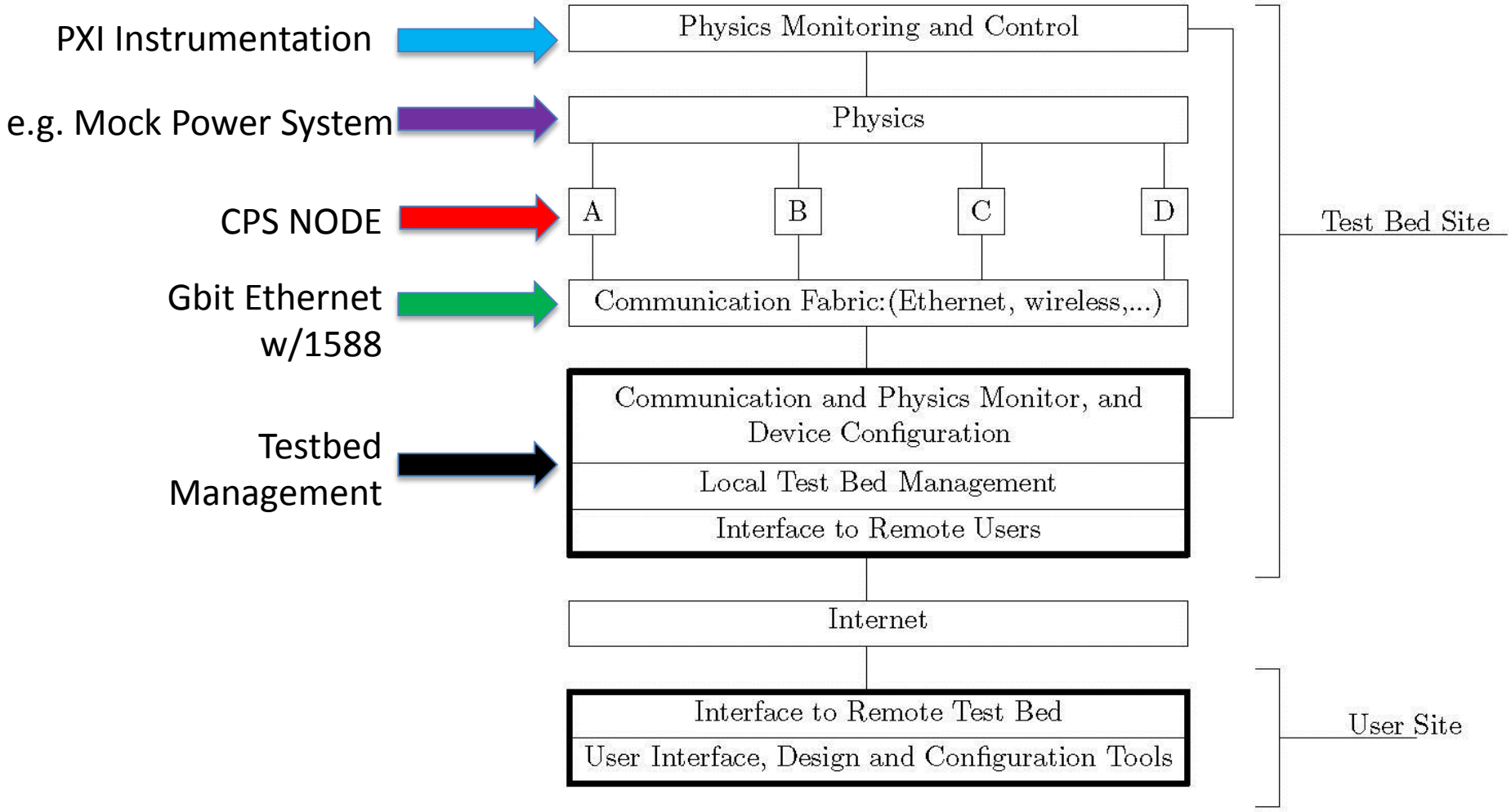
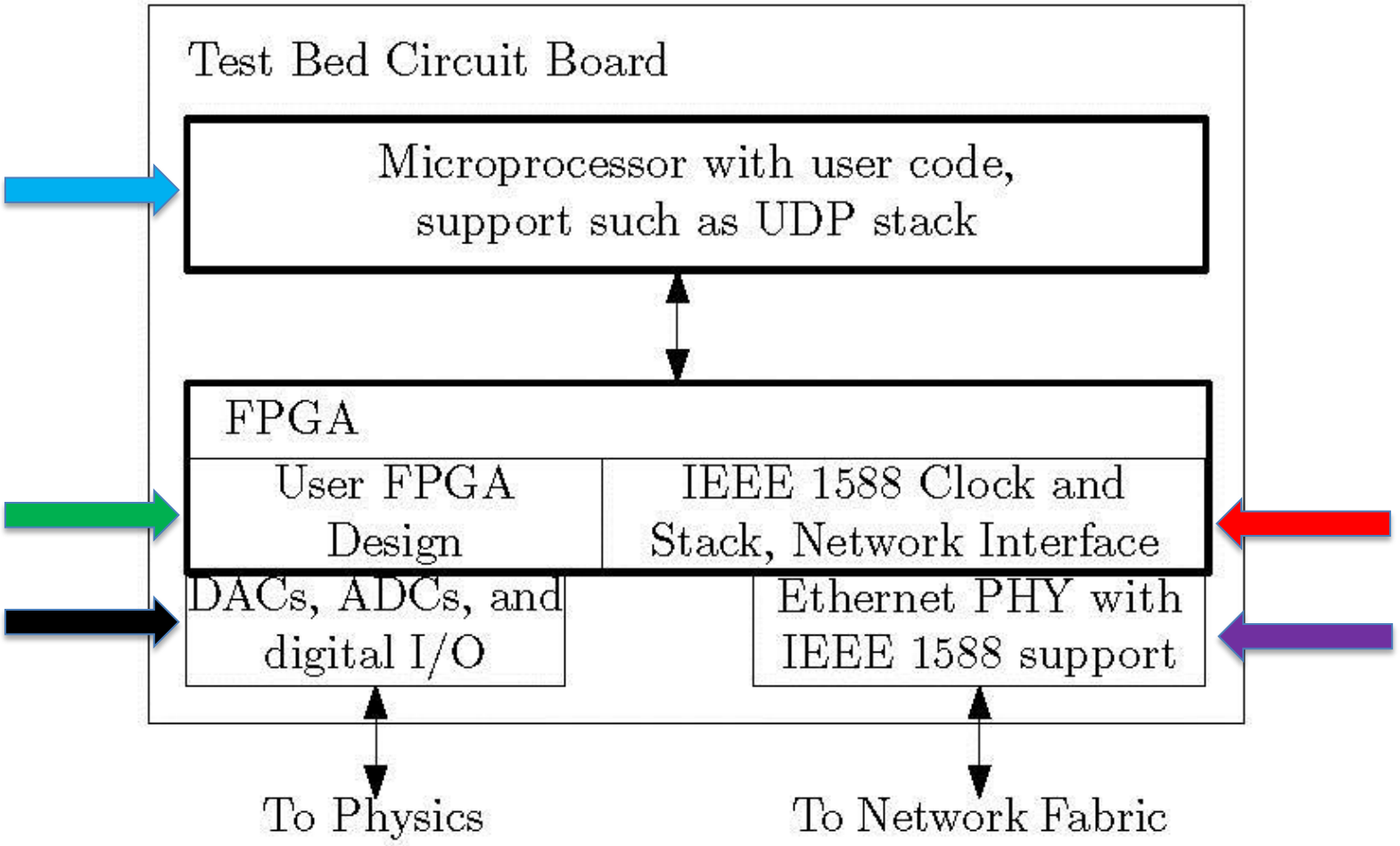
The purpose of the “correct-by-construction” timing testbed is to:

- Facilitate R&D, proof of concept, and collaboration in timing methodologies and design environments
- Allow comparison and verification of design alternatives.
- Explore metrics and test methods

# Testbed Architecture



# Testbed CPS Node Architecture



# The Testbed "Hello World" examples

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To shorten the learning curve in using the testbed we propose two hello world examples:

- A time triggered implementation
- A Ptides implementation

Both will implement the same application-tentatively measuring and adjusting the phases of two legs of a mock power grid prior to interconnection.

# Conclusions

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- There is still a lot of work to do before we have correct-by-construction timing
- The proposed testbed will enable more rapid progress particularly in the areas of:
  - Designs for hardware support of explicit time,
  - Designs for true real-time operating systems,
  - Languages, compilers, and other software development infrastructure,
  - Techniques for exploiting explicit time in applications.

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# Thanks for your attention!