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Performance of Assisted Partial Timing Support (APTS)

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Introduction

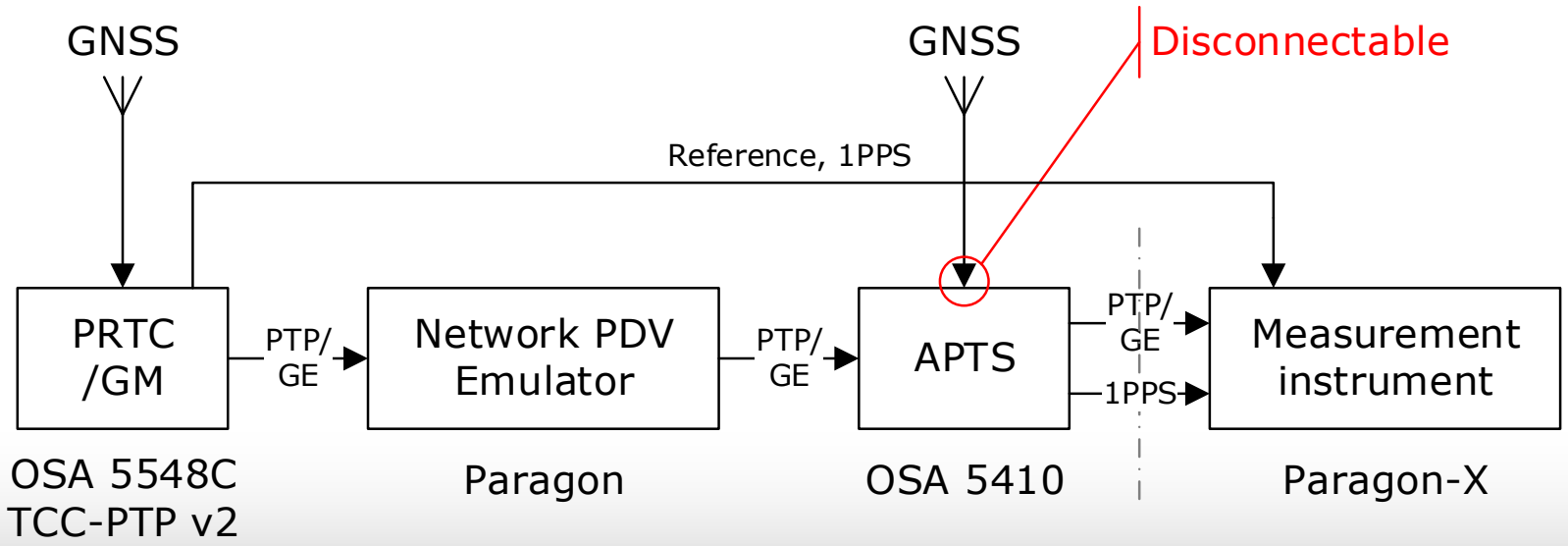
Objectives of the tests:

- Study performance potential of APTS
- Compare several ways of locking to the back-up GM
- Draw conclusions for the architecture

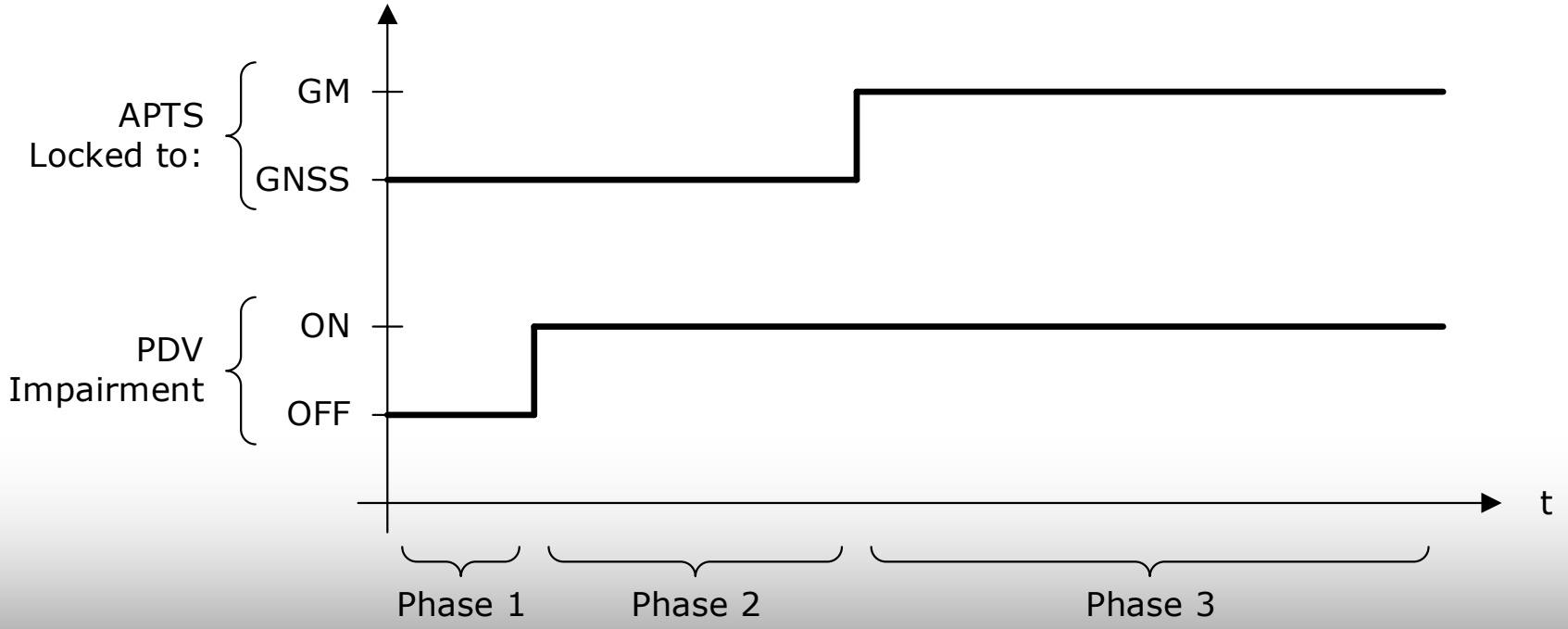
Method

- Emulate PDV of the network
- Measure TE at output of the APTS Clock before and after protection event (GNSS failure)

Test setup



Test sequence

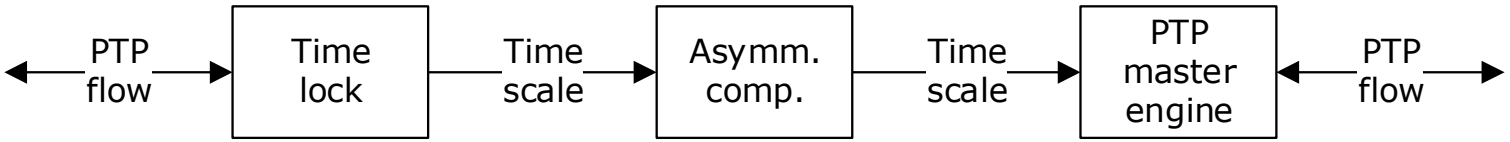


Two APTS mechanisms

1. Normal condition: locked to GNSS

   Simultaneously: slave port time-locked to Core GM and measurement of delay asymmetry

   Failure condition: time-lock to Core GM and delay asymmetry compensation



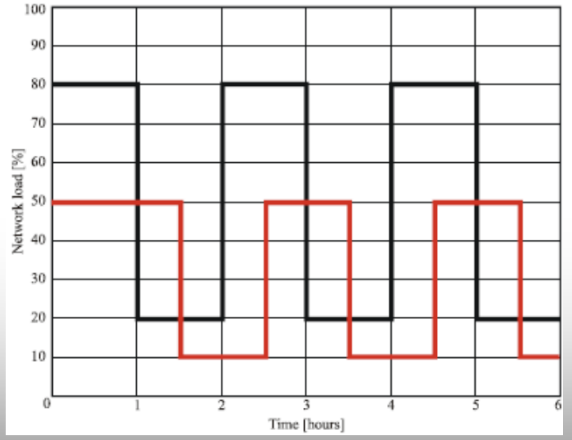
2. Normal condition: locked to GNSS

   Simultaneously: slave port frequency-locked to Core GM

   Failure condition: frequency-lock to Core GM; time clock continues ticking with this frequency

Three PDV impairment cases

1. A static delay asymmetry between forward and reverse directions of 10 µs
2. G.8261/VI test case 12, traffic model 1[1]:
   - 80% traffic load in forward direction over 10 nodes
   - 20% traffic load in reverse direction over 10 nodes
3. G.8261/VI test case 13, traffic model 1[1]:
   - Sudden load changes
   - **Black**: forward direction (10 nodes)
   - **Red**: reverse direction (10 nodes)



Note 1: using Calnex reference PDV traces

Summary of test cases

Test #	APTS mode	PDV impairment profile
1	Lock time via PTP transfer, asymmetry compensation	10 µs static delay asymmetry
2	Idem	G.8261/VI test case 12, traffic model 1[1]
3	Idem	G.8261/VI test case 13, traffic model 1[1]
5	Hold time via PTP frequency transfer	10 µs static delay asymmetry
6	Idem	G.8261/VI test case 12, traffic model 1[1]
7	Idem	G.8261/VI test case 13, traffic model 1[1]

Measurements

What is being measured?

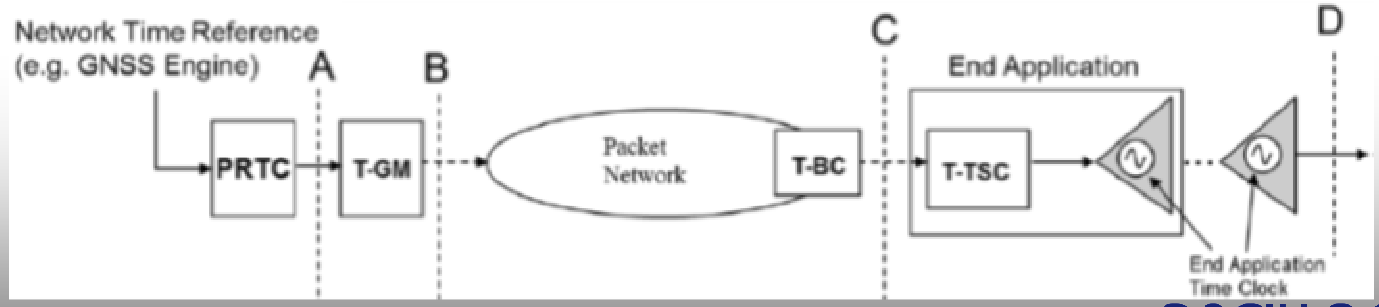
- Time Error TE of the outgoing two-way PTP stream, i.e. avg(TE_{T1}, TE_{T4})

What is being calculated?

- max |TE|, MTIE

What are the results compared against?

- Network Limits @ reference point C, G.8271.1, Amd1, § 7.3



Discussion

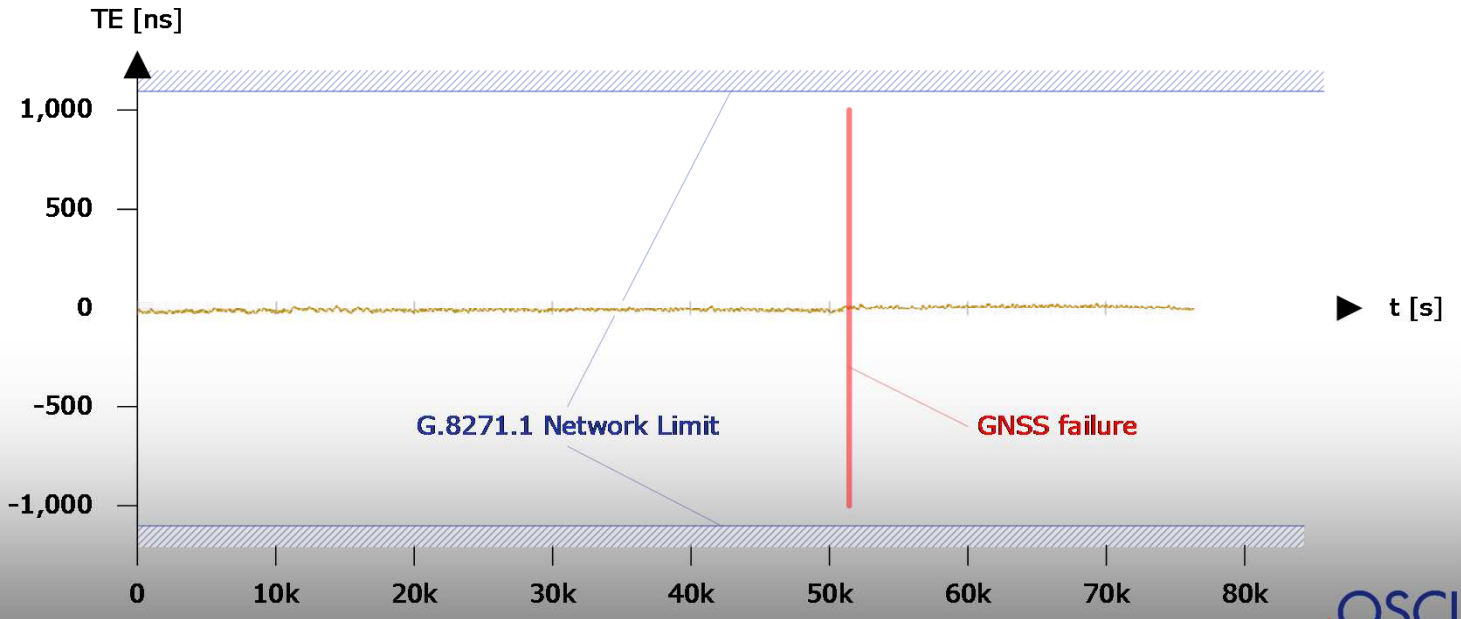
- Are the PDV traces emulating G.8261/VI test cases the right ones for evaluating APTS?
- Questionable, because G.8261/VI is for a network without timing support from the network; consequence: the test is actually too tough on the tested APTS function
- Are the Network Limits of G.8271.1 the right ones for evaluating APTS?
- No (formally), because G.8271.1 is for the case of full timing support from the network; G.8271.2 will specifiy network limits for the case of partial timing support, both assited and non-assisted; but it is not yet finalized.
- Yes, because: why should the network limit at reference point C be any different in the case of assisted partial timing support?

Note 1: Calnex bi-directional reference PDV traces

Test #1, Time Error

Static asymmetry of 10 µs, APTS = phase lock & asymmetry compensation

max|TE| = **38 ns** ≤ 1100 ns



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Test #1, Time Error

Static asymmetry of 10 µs, APTS = phase lock & asymmetry compensation

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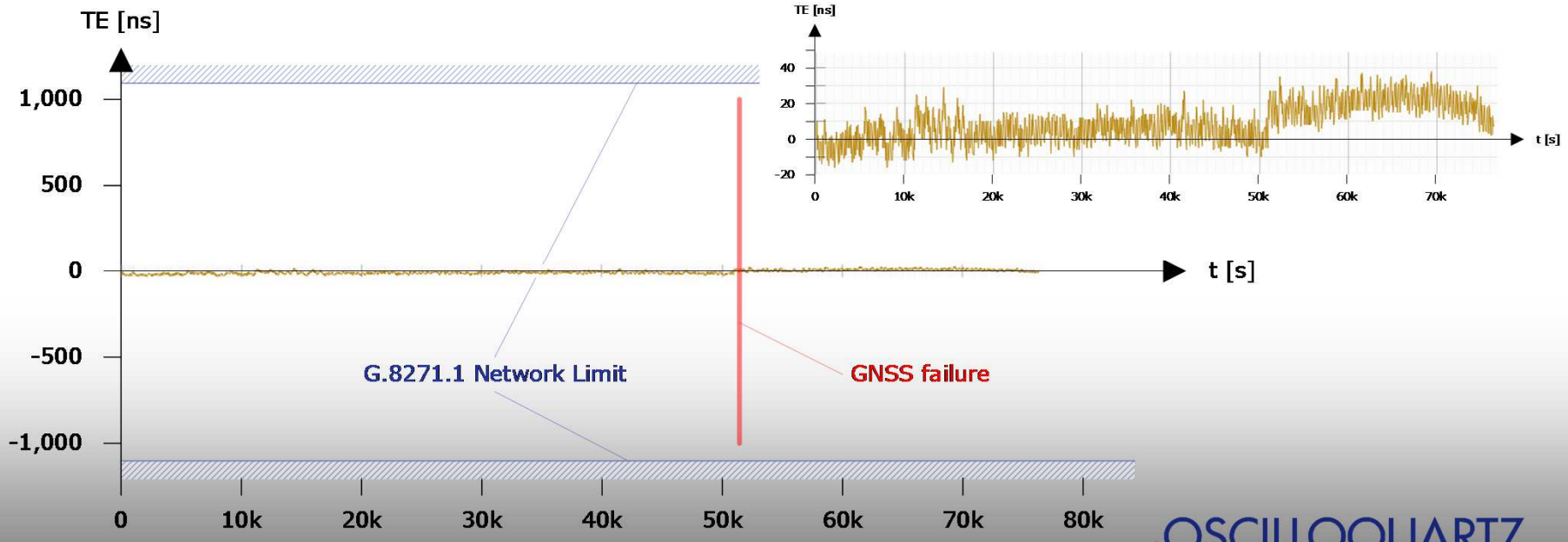

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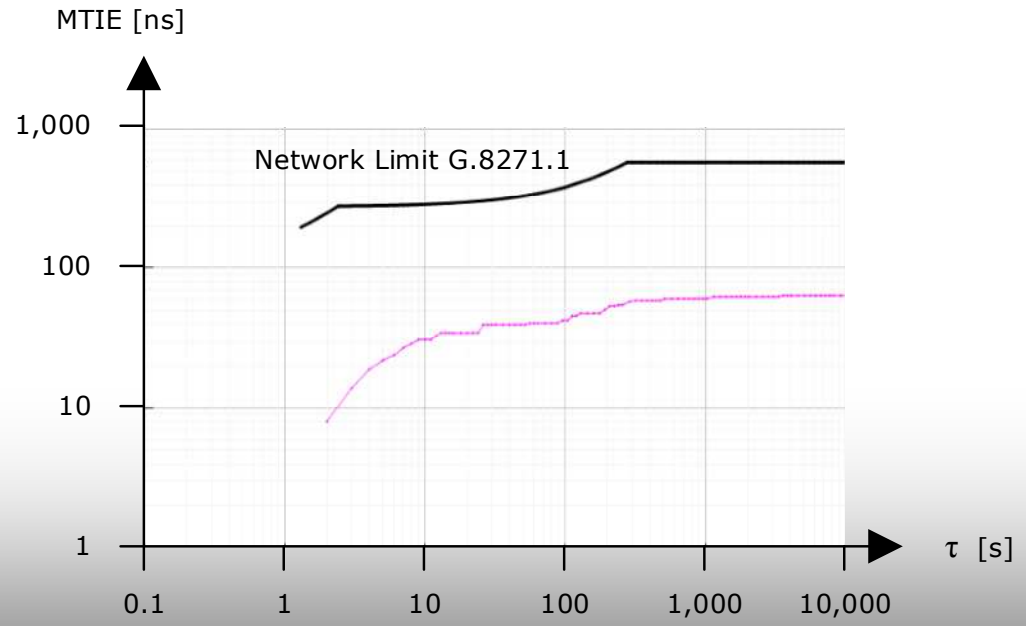
Test #1, MTIE (dynamic Time Error)

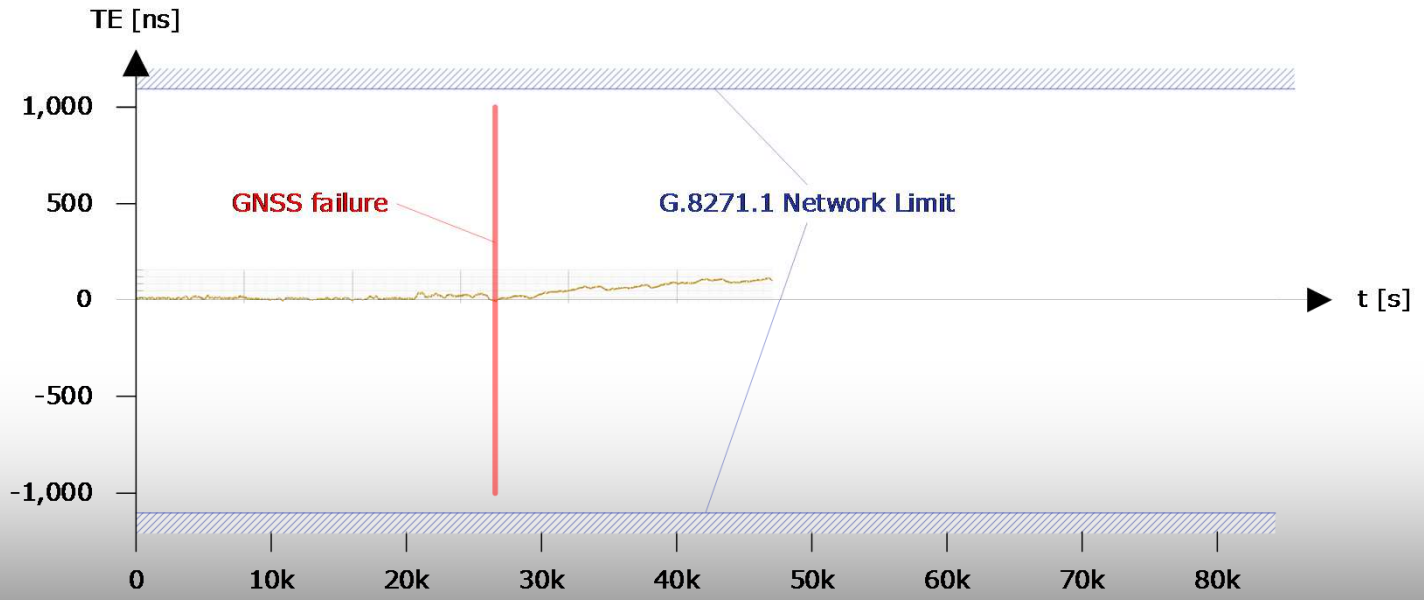
Static asymmetry of 10 µs, APTS = phase lock & asymmetry compensation



Test #2, Time Error

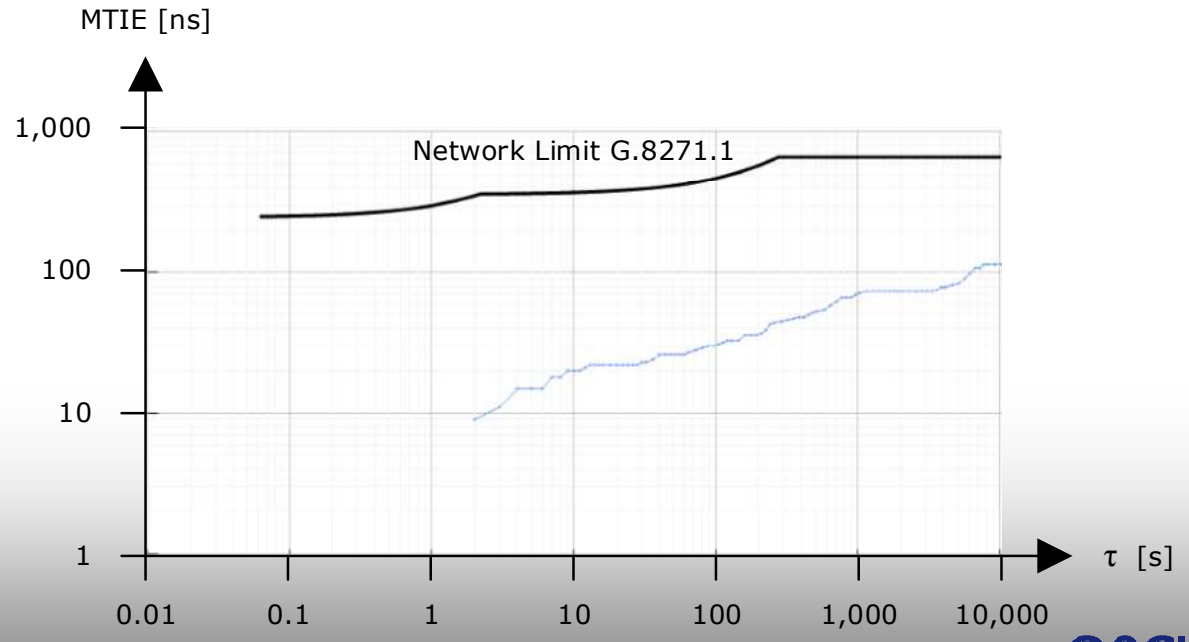
G.8261/VI test case 12-1, APTS = phase lock & asymmetry compensation

max|TE| = **116 ns** ≤ 1100 ns



Test #2, MTIE (dynamic Time Error)

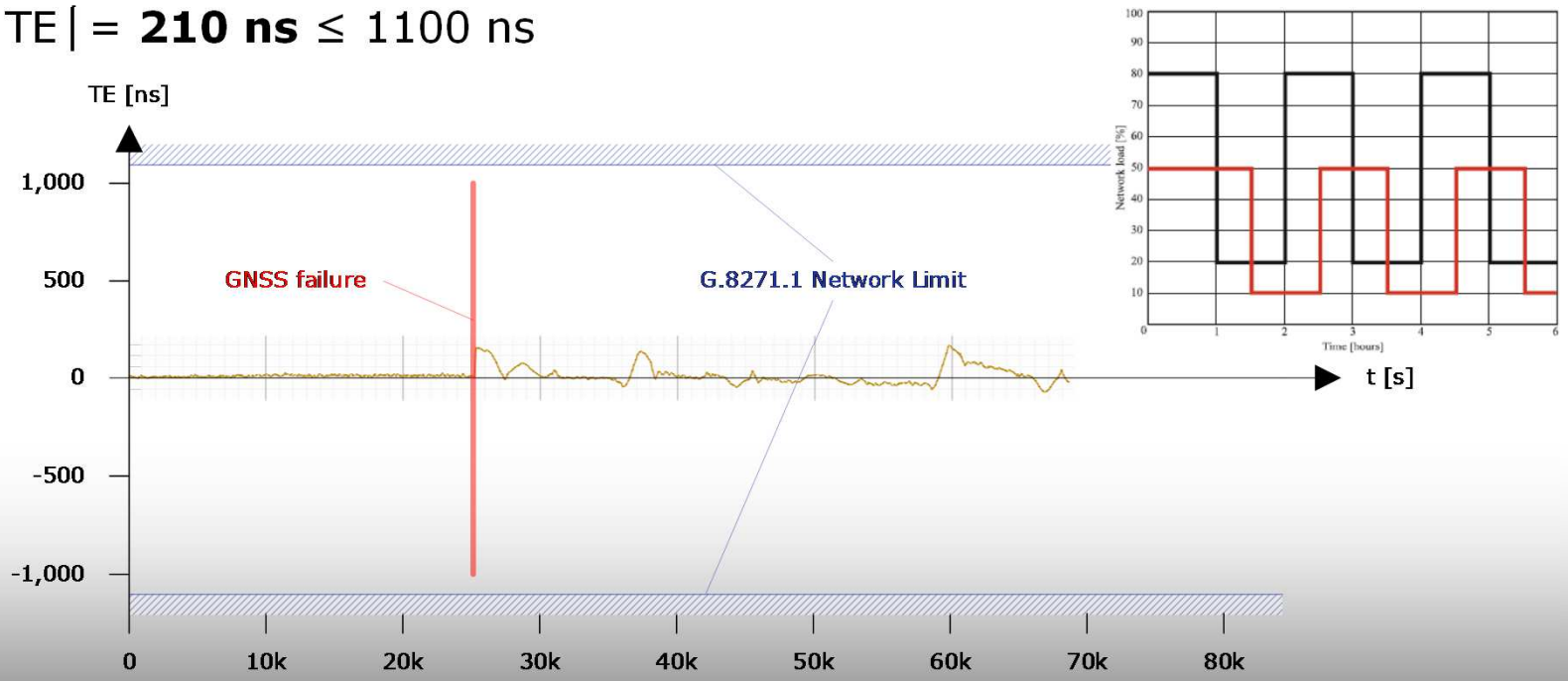
G.8261/VI test case 12-1, APTS = phase lock & asymmetry compensation



Test #3, Time Error

G.8261/VI test case 13-1, APTS = phase lock & asymmetry compensation

max|TE| = **210 ns** ≤ 1100 ns



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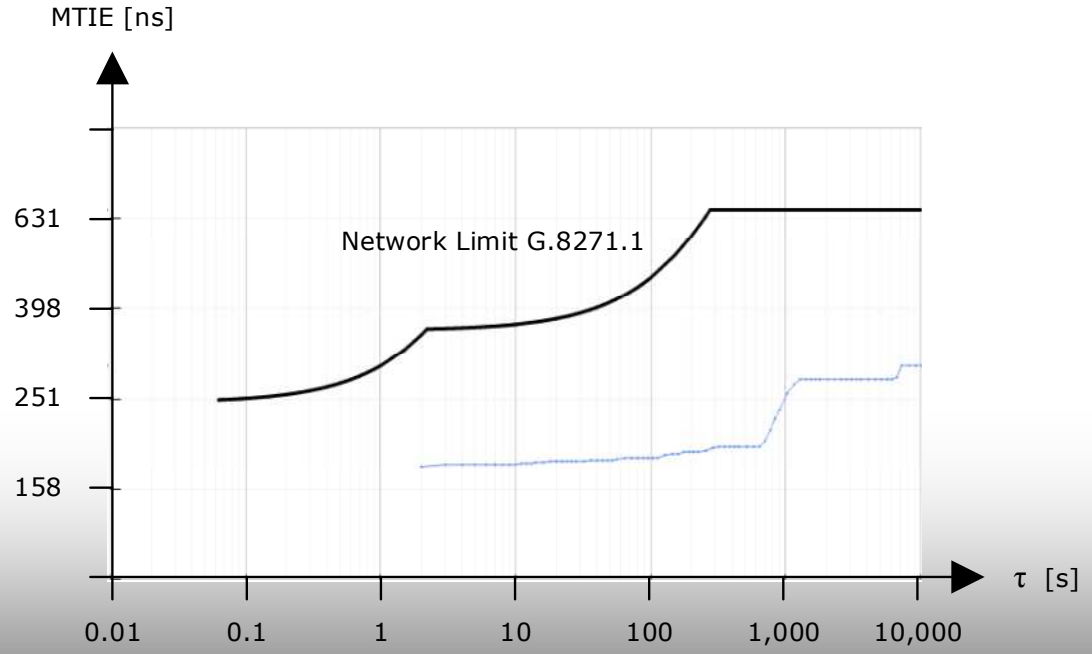
Test #3, MTIE (dynamic Time Error)

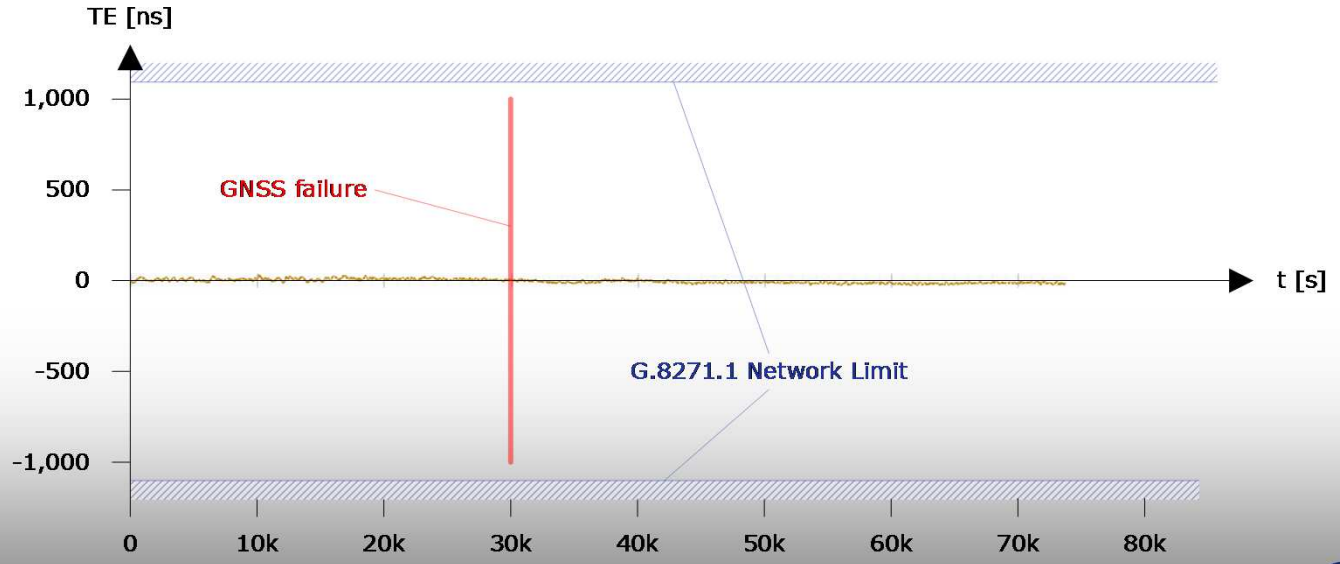
G.8261/VI test case 13-1, APTS = phase lock & asymmetry compensation



Test #4, Time Error

Static asymmetry of 10 µs, APTS = frequency lock

max|TE| = **36 ns** ≤ 1100 ns



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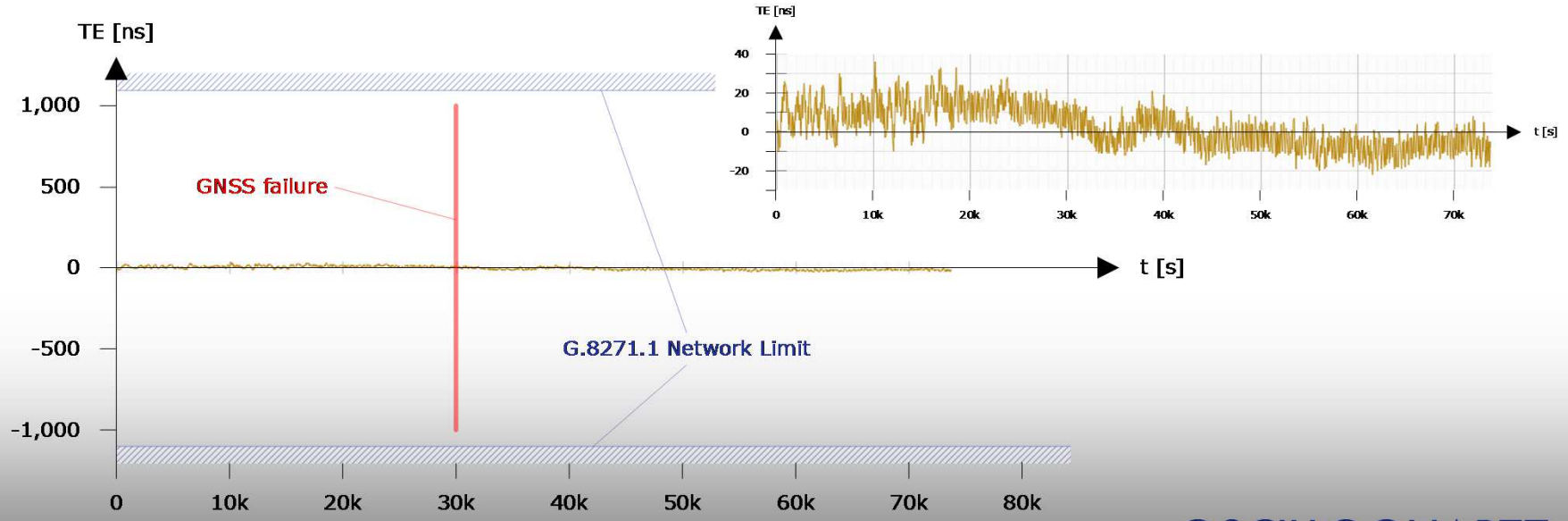
Test #4, Time Error

Static asymmetry of 10 µs, APTS = frequency lock

max|TE| = **36 ns** ≤ 1100 ns



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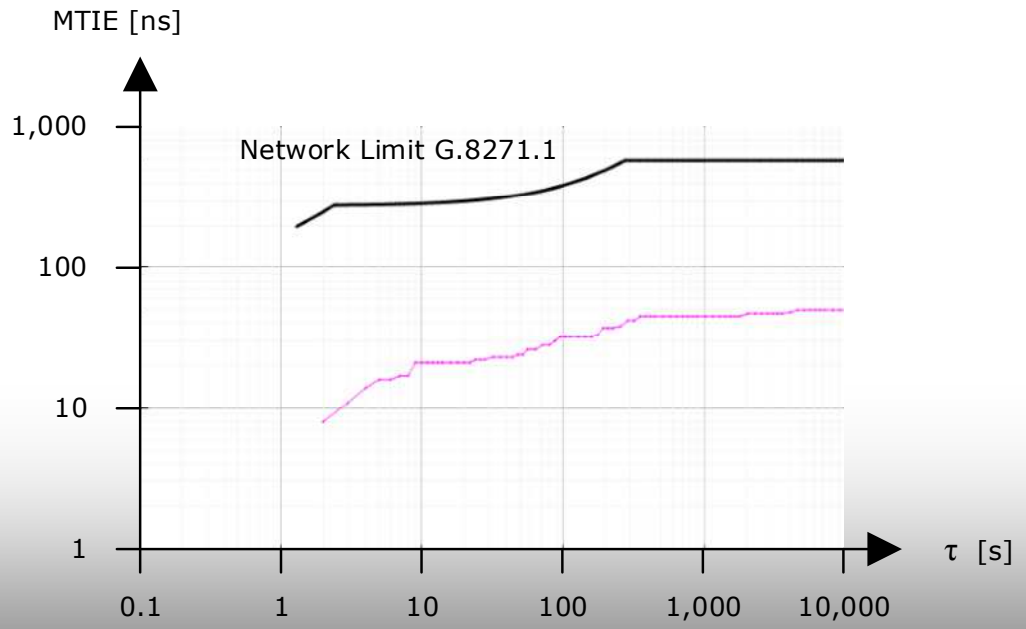
Test #4, MTIE (dynamic Time Error)

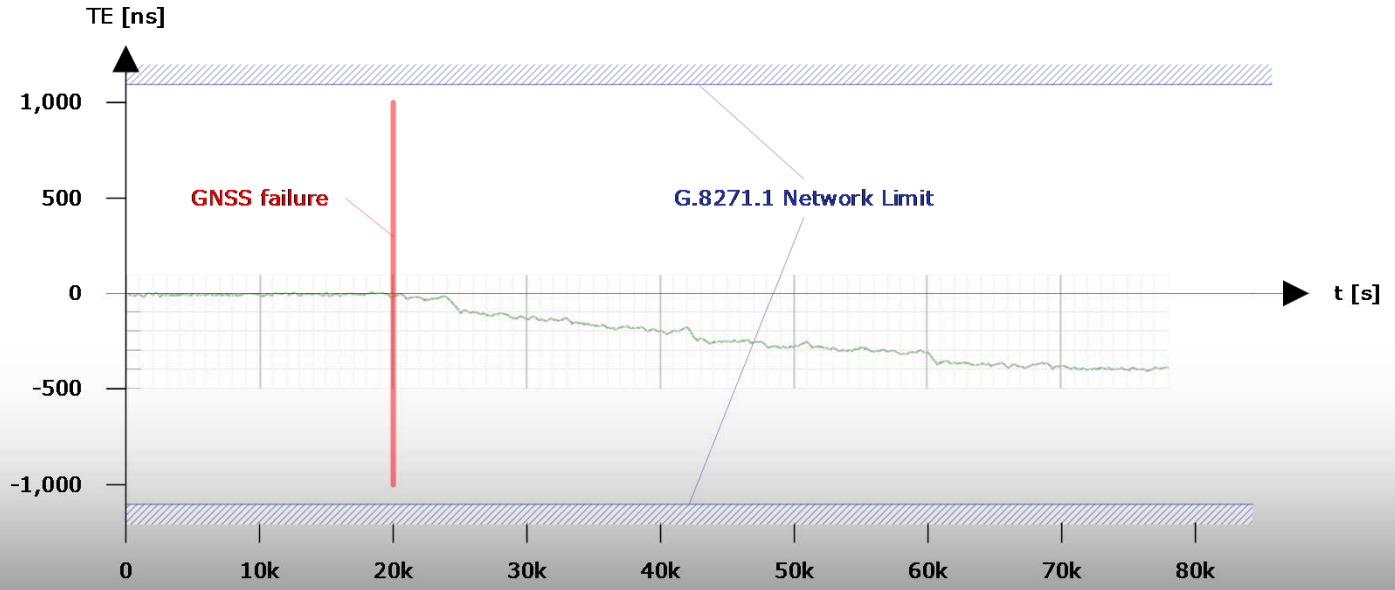
Static asymmetry of 10 µs, APTS = frequency lock



Test #5, Time Error

G.8261/VI test case 12-1, APTS = frequency lock

max|TE| = **410 ns** ≤ 1100 ns



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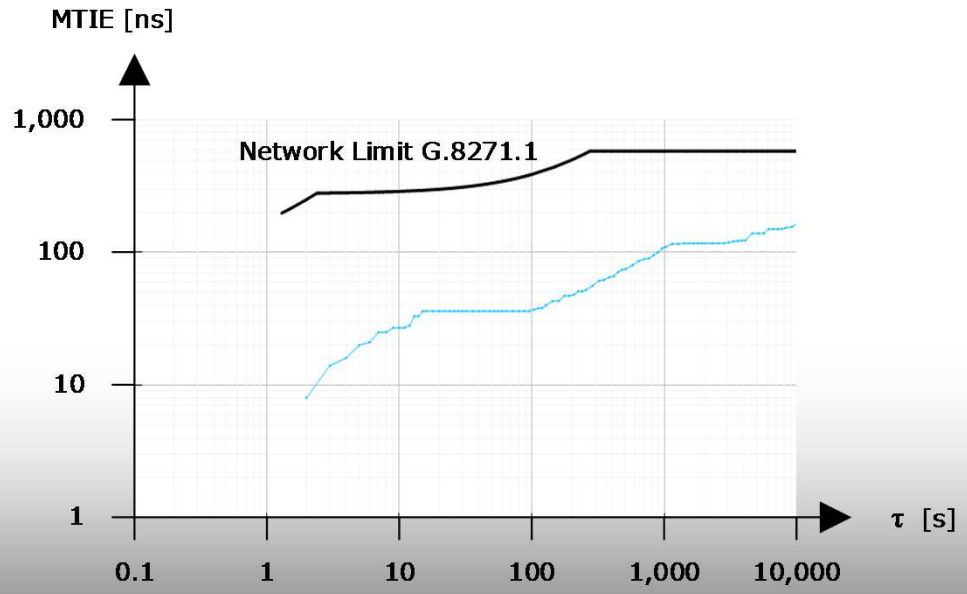
Test #5, MTIE (dynamic Time Error)

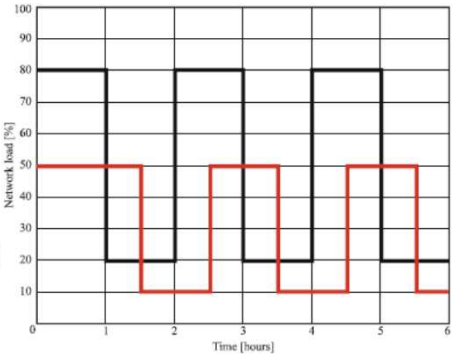
G.8261/VI test case 12-1, APTS = frequency lock

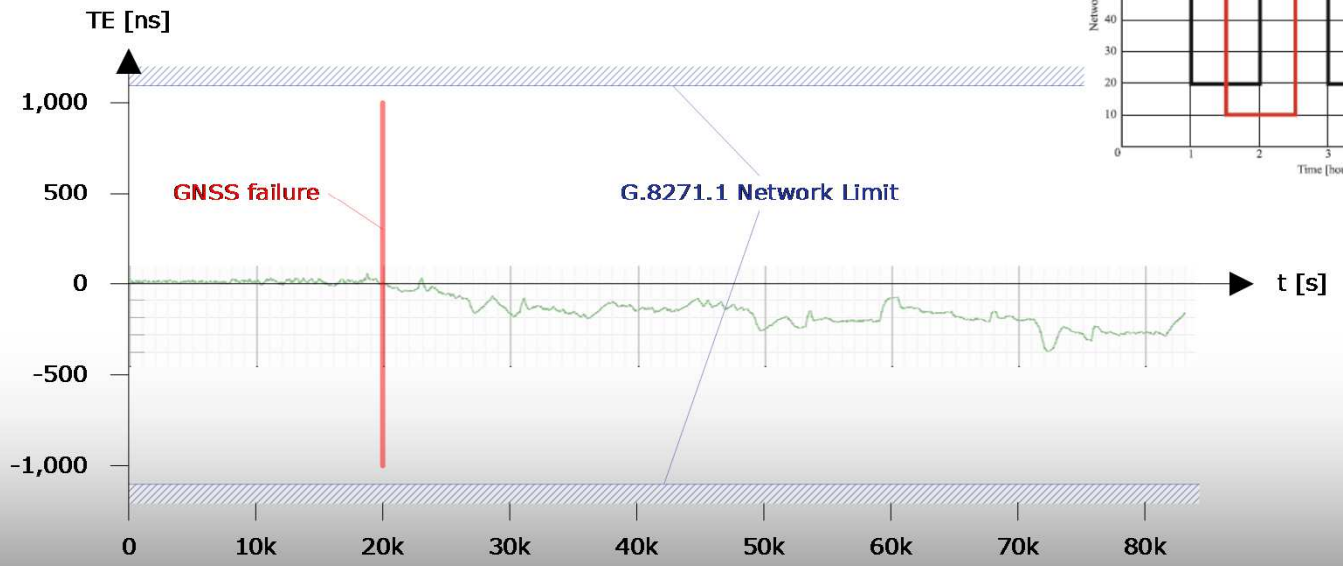


Test #6, Time Error

G.8261/VI test case 13-1, APTS = frequency lock

max|TE| = **356** ns ≤ 1100 ns





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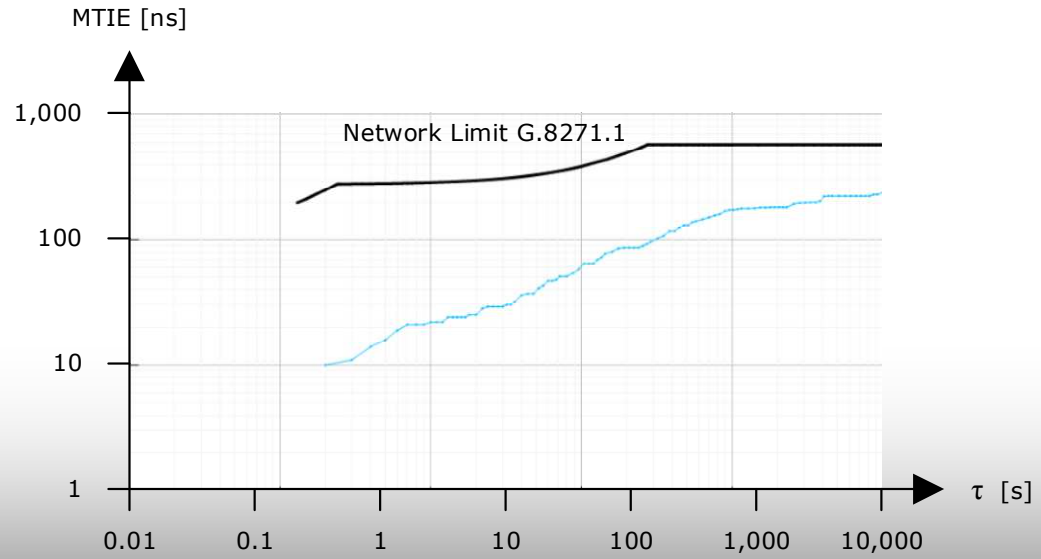
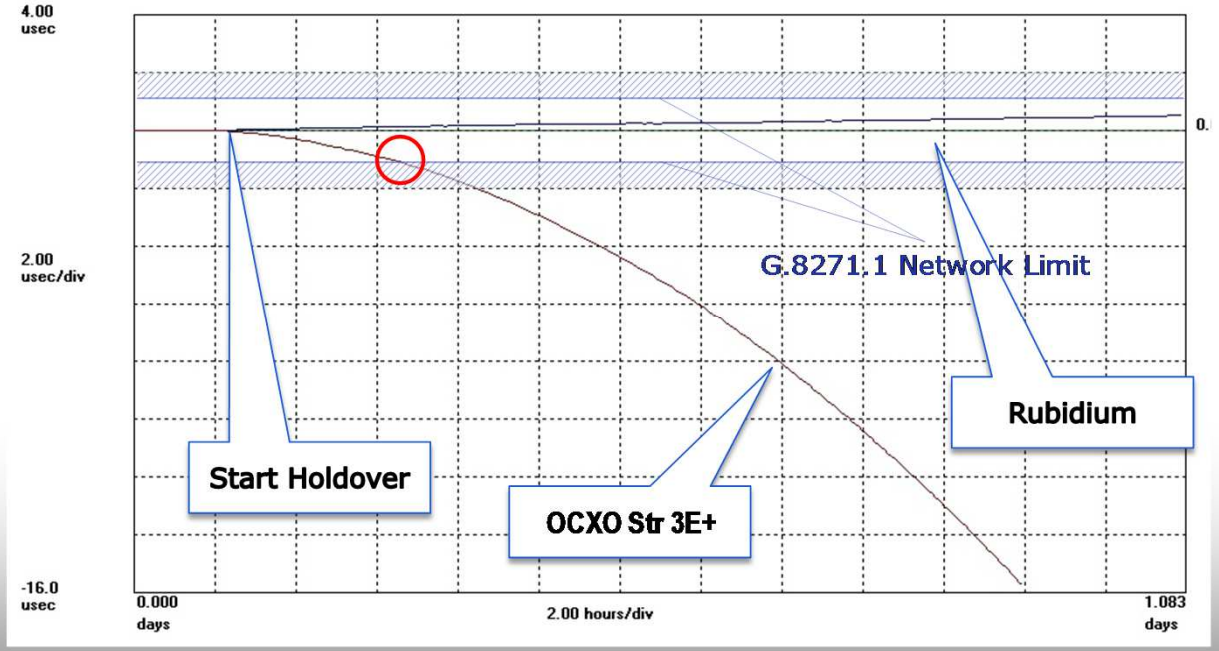
Test #6, MTIE (dynamic Time Error)

G.8261/VI test case 13-1, APTS = frequency lock

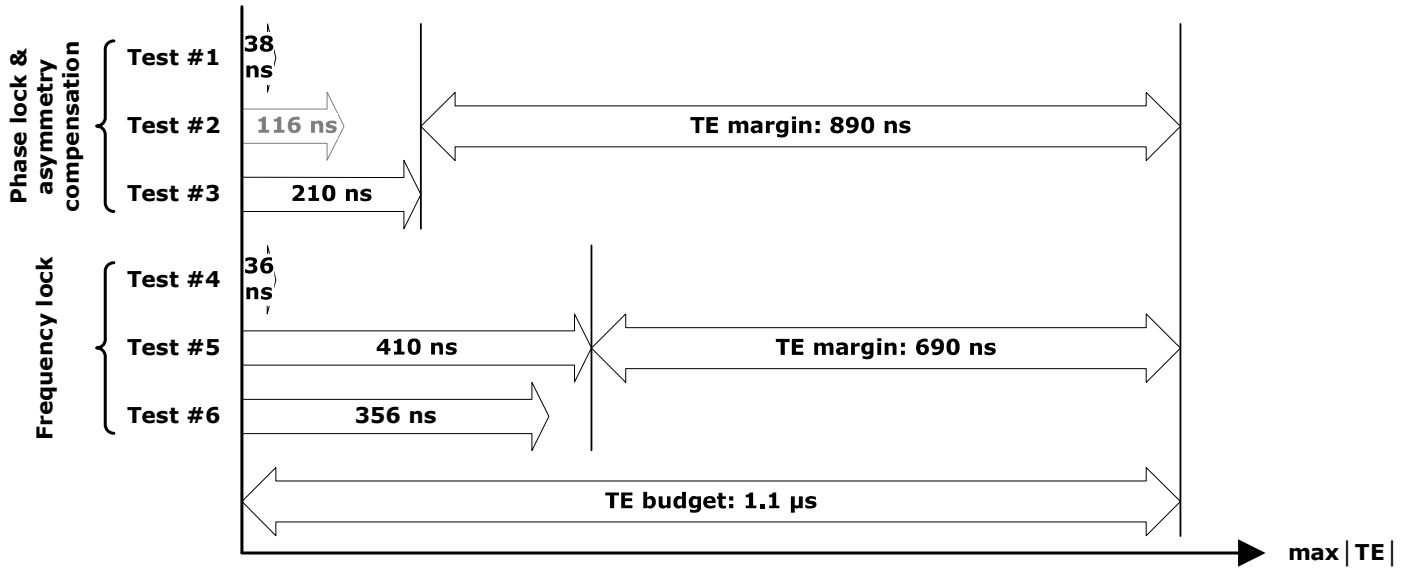


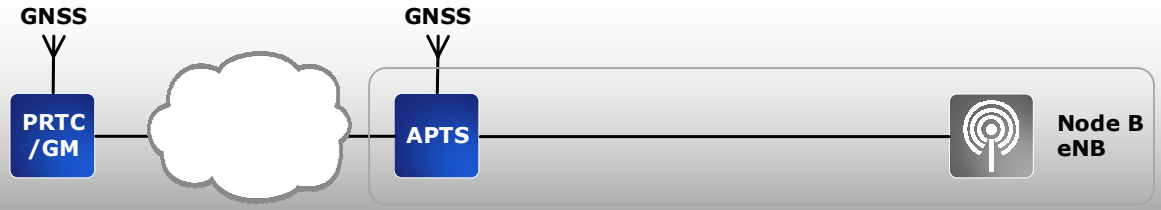
Compared with holdover …

- Holdover (XO & Rb), ideal conditions (temperature, initial offsets):

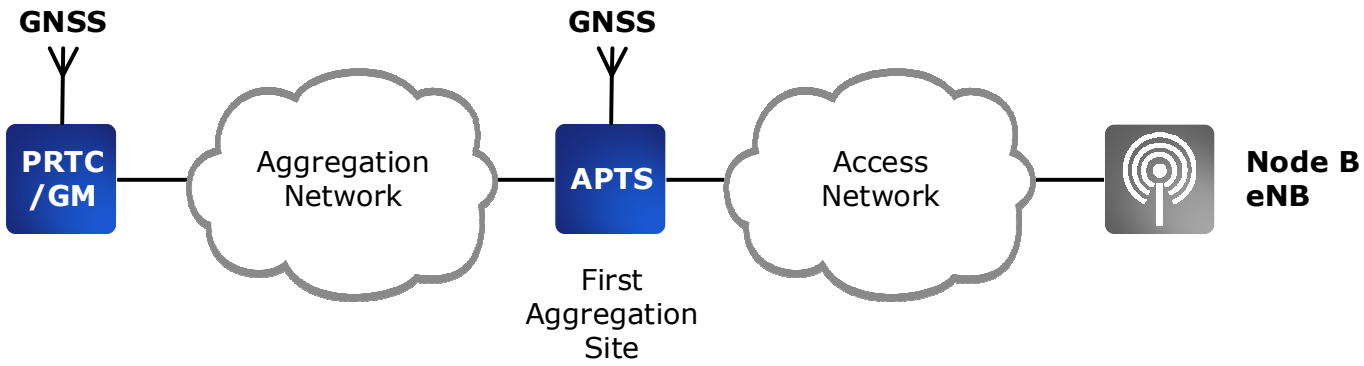


Summary





Conclusion



- Tests based on G.8261 test cases (!) show that the max|TE| at the output of the APTS Clock is well below the 1.1 µs in the GNSS failure case.
- The test results suggest that the APTS Clock can be placed in the first aggregation site.
- With the PDV emulations used, phase lock with asymmetry compensation fares somewhat better than frequency lock, but this probably depends on the test and network conditions.
- The results depend on the algorithms used in the APTS Clock.
- APTS is better than quartz-based holdover.

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Thank You