Runtime Measurement of Latency at ps Level in Serial Links

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Agenda

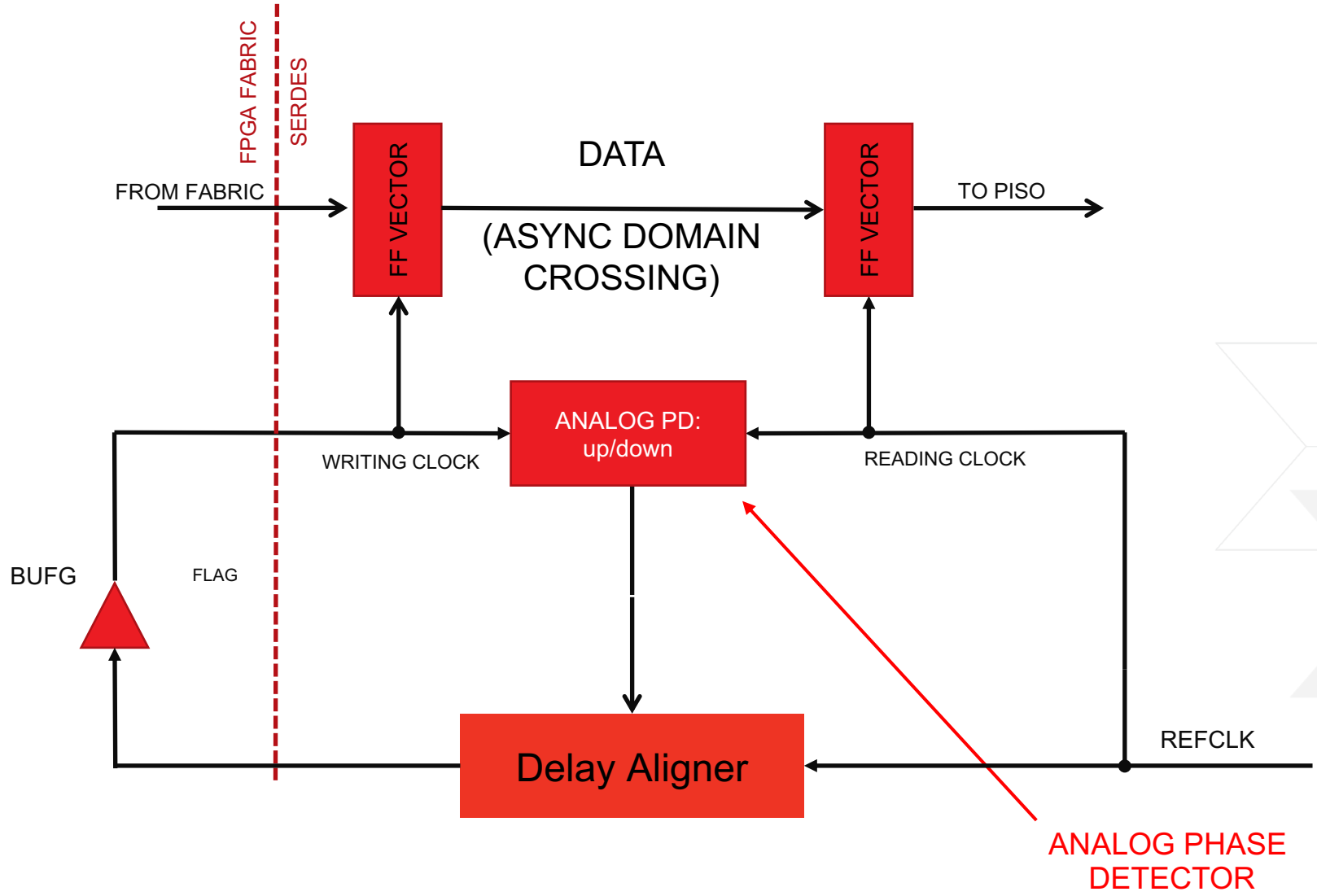
- **The Challenge in IEEE1588**
  - From the Transceivers Standpoint
- **Controlling the latency**
  - A good idea
  - Architecture 1 and 2
- **Measuring the latency**
  - A better idea
  - Architecture 3
- **Conclusions**

The Challenge in IEEE1588

- **Many Electronics blocks have a latency defined in clock cycles.**
- **Some key building blocks have an “analog” latency, defined in ps.**
  - FIFOs.
- **FIFO Latency is not fixed:**
  - Temperature
  - Power supply level
  - Silicon process

In General, a Serdes Changes Latency at Each Startup and During Operation.

Controlling The Latency: Fifo Bypass Architecture



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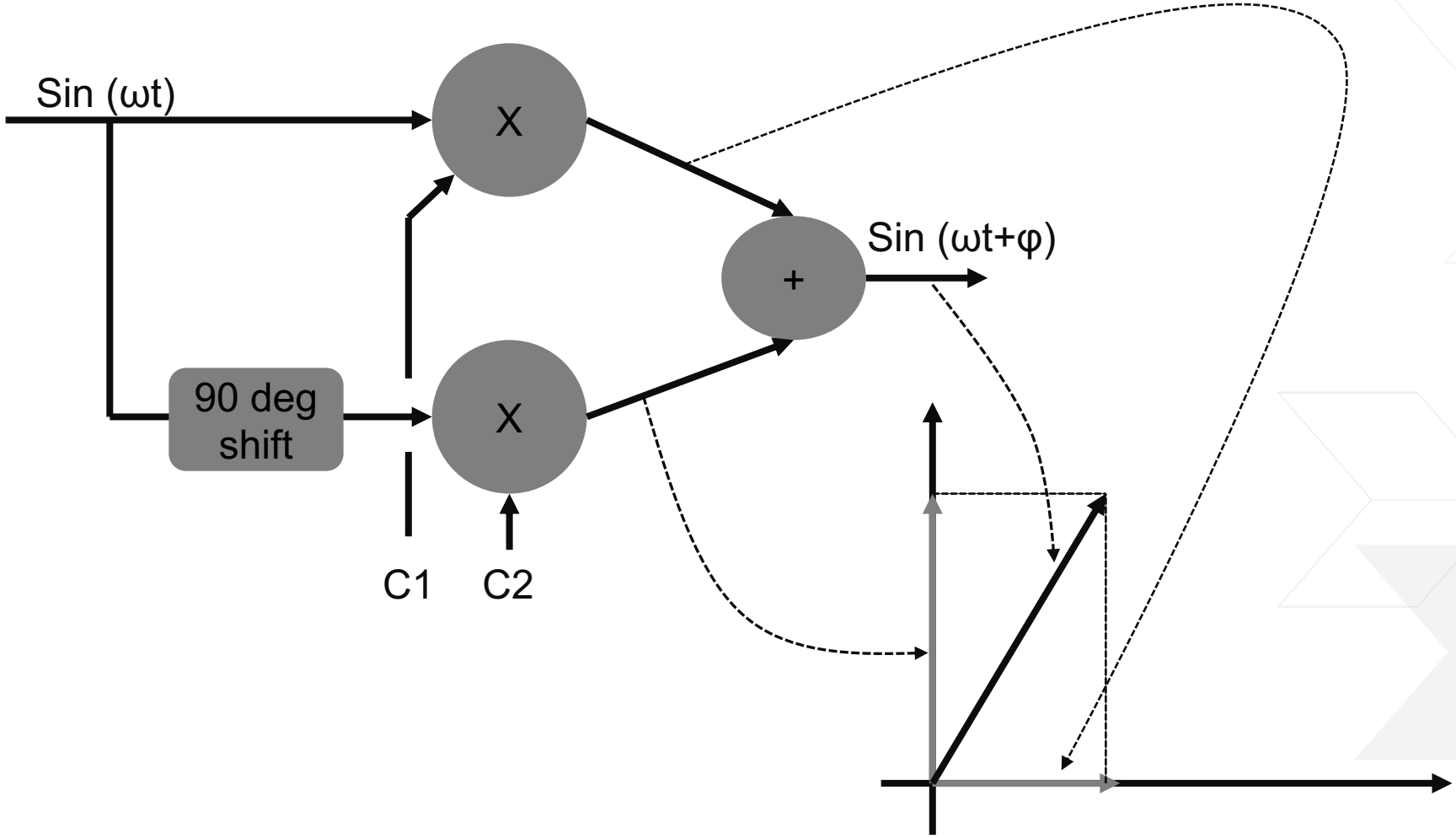
Controlling The Latency: Fifo Bypass Architecture

- **Achieves minimum absolute latency**
  - Bypasses the FIFO completely
  - Most popular feature for Fintech HFT (High Frequency Trading)
- **Latency is set and maintained over time**
  - Precision is dictated by PD implementation, clocktree etc.

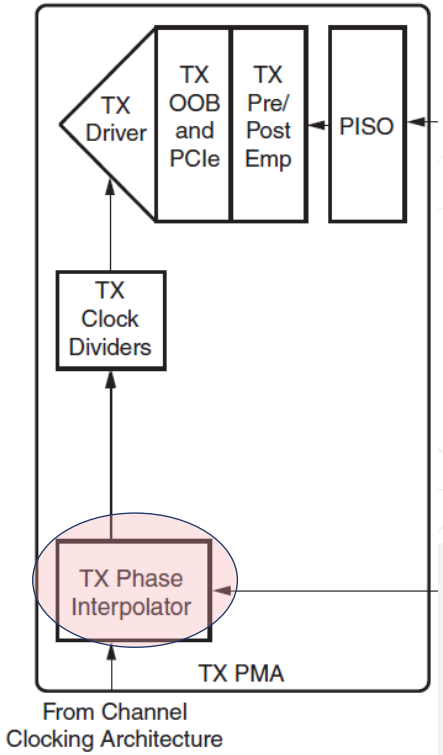
Phase Interpolator: Infinite Delay Line



Unbounded Phase Shift Possible!

TX and RX Phase Interpolator

- **Each Receiver has its own Phase Interpolator**
  - Traditionally managed by the CDR logic
  - Can be manually controlled
  - Equivalent to ADC 1bit with fine phase control.
- **Each TX Serdes has its own Phase Interpolator**
  - Can shift the TX phase back/forward in steps of 1UI/32
  - Infinite shift allowed
  - A continuous shift emulates a frequency change
- **This can work on top of the fractional PLL.**
  - A TX serdes can be used as a fractional VCXO, with digital control.



Fine Unbounded Phase Shift = Frequency Shift.

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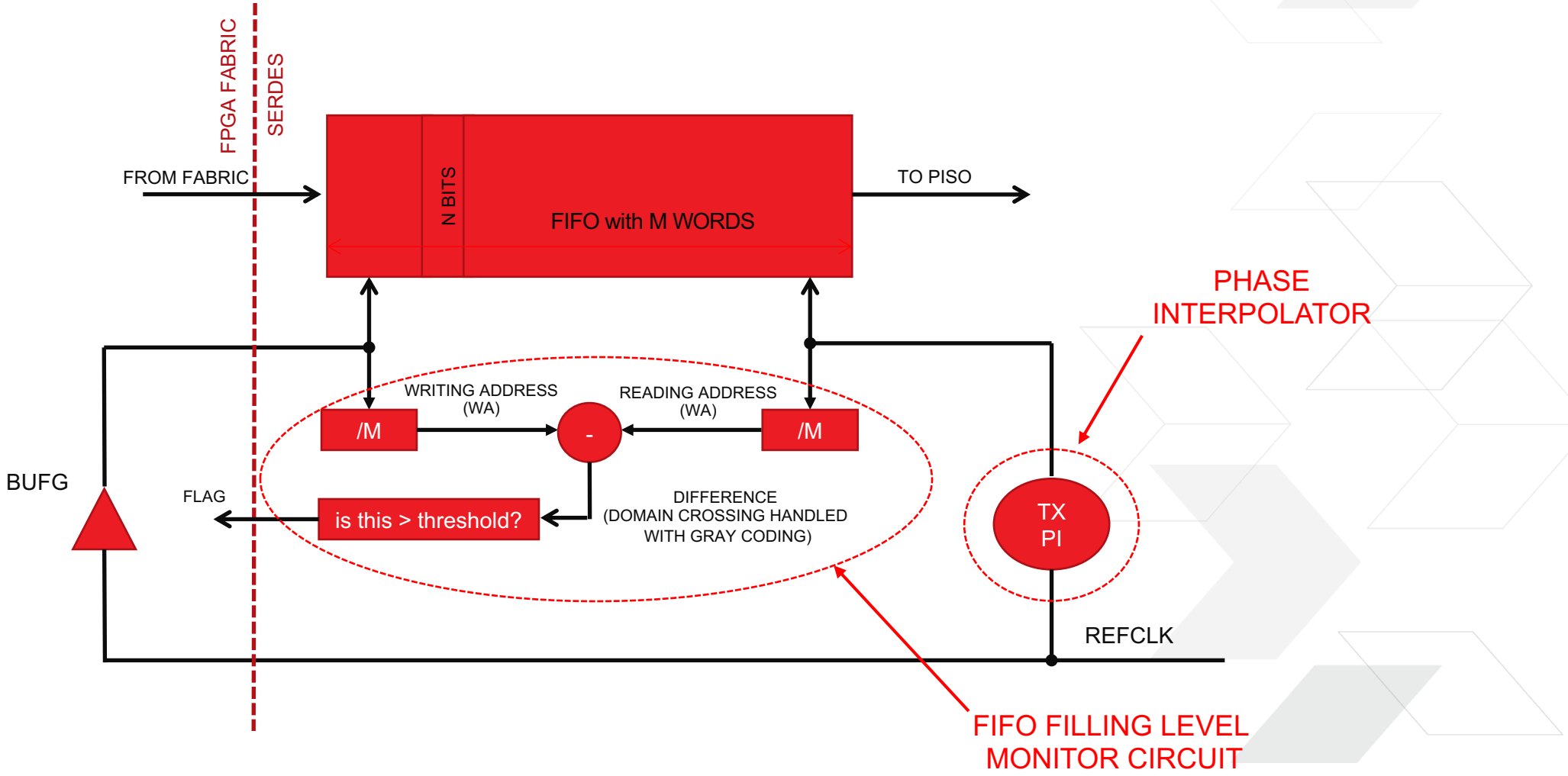
Latency Control Architecture



Controlling The Latency

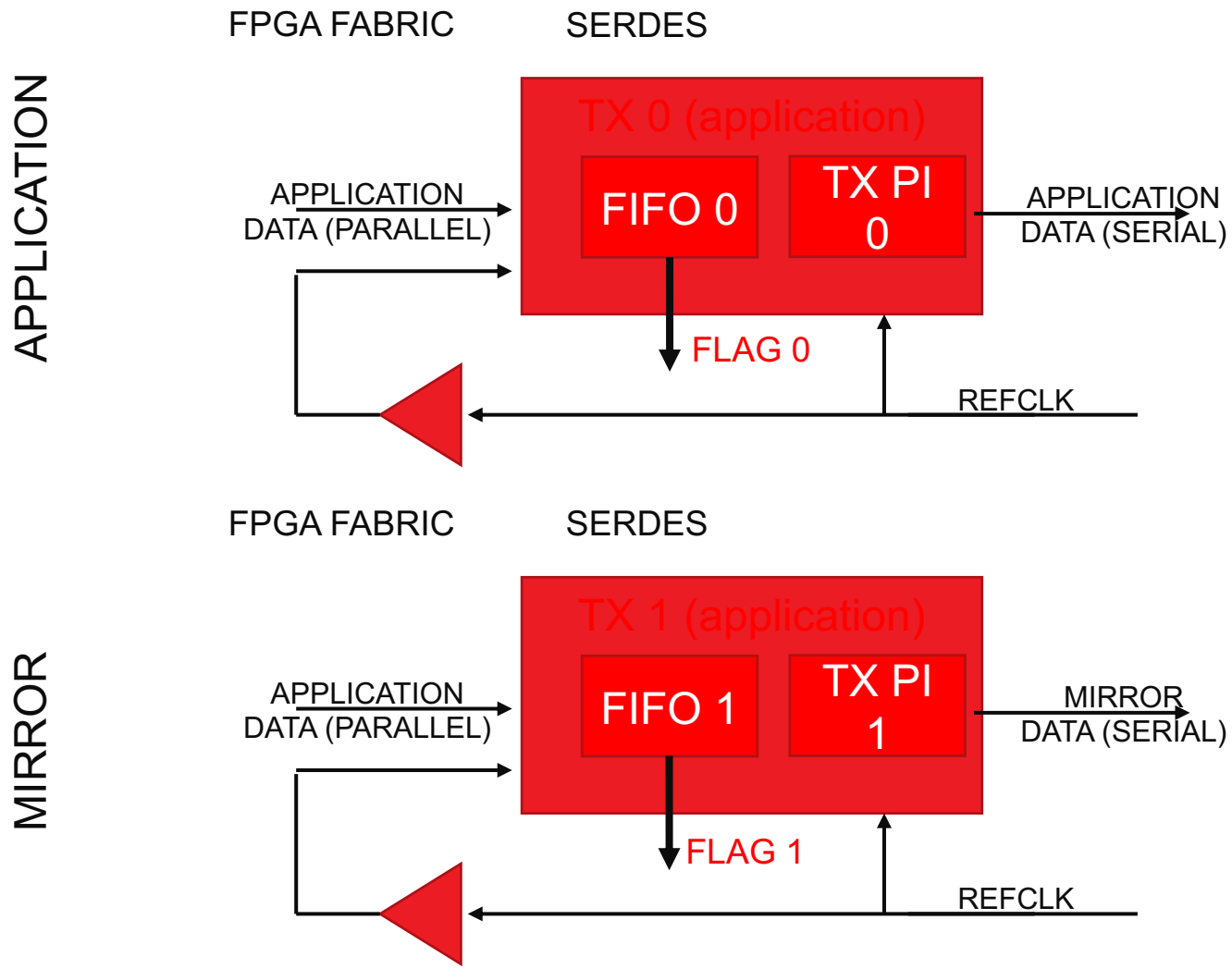
- **Achieves and maintains the FIFO at half of its latency**
  - Latency is not as low as the previous case.
- **Latency is set and maintained over time**
  - The way the flag is filtered dictates the precision of the latency.
  - Latency can be controlled in a much more precise way than buffer bypass.

Alternative Approach: Measuring the Latency

- **We do not want to control the latency**
  - Latency across a FIFO is not controlled or constrained.
  - This latency will change with PVT
- **We want to measure the latency, continuously**
  - We correct the time stamp “mathematically”

Measuring the Latency by Using a Mirror Structure

TX Latency Measured on a «Mirror» Structure



Multiple transmitters share PVT

How can I equalize their latency?

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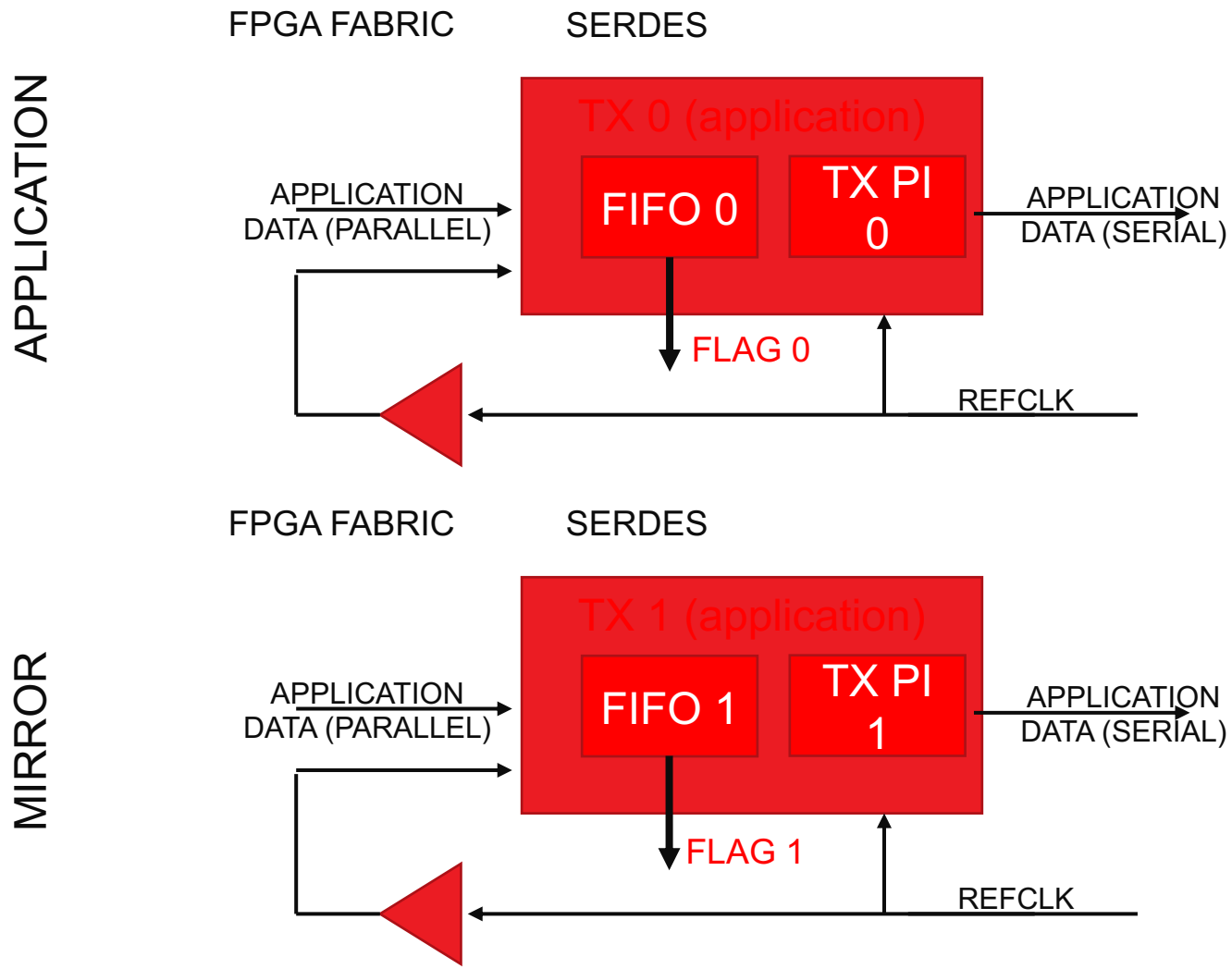
TX Latency Measured on a «Mirror» Structure



- At the beginning, both serdes are set for half their latency
- During application, the latency will change according to PVT and the mirror serdes will track the application serdes
- In the mirror, I can step the PI and count how many steps I need to bring it back to the half full condition

- Latency can be masured with the resolution of the PI (1 ps)
- This value can be used to «correct» the hw TS

Conclusions

- **Two different approaches to cope with the serdes latency have been presented:**
  - Constraining the latency
  - Measuring the latency
- **A set of building blocks are devoted to precise phase/latency control and measurement.**

Adaptable.
Intelligent.

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